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Analysis of Thermal Treatment Zirconia as Spacer Layer on Dye-Sensitized Solar Cell (DSSC) Performance with Monolithic Structure

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Abstract

Monolithic Dye-Sensitized Solar Cells (DSSC) offers the prospect of lower material cost and require a simpler manufacturing process compared to the conventional DSSC. This device is fabricated on a single Fluorine Tin Oxide (FTO) glass substrate that consists of a nanoporous TiO_2 photoanode layer, a ZrO_2 spacer layer, a carbon counter electrode layer, a dye, and an electrolyte. The spacer layer on the monolithic DSSC serves as electrolyte storage and the insulating layer to separate between photoanode and the counter electrode. Zirconia (ZrO_2) is often used as a spacer because it has high temperature resistant, high dielectric constant and has a band gap between 5-6 eV. In this work, the effects of the thermal treatment of the zirconia layer as a spacer layer on the performance of monolithic DSSC have been investigated. The cell's performance increases with the sintering temperature as well as indicated by the decrease in particle size. Co-sintering treatment with carbon counter electrode layer tends to reduce the cell's performance drastically. The highest performance was obtained at a sintering temperature of 500 ^oC with a PCE of 0.22%, I_{sc} = 0.16 mA and V_{oc} = 0.71 V.

Keywords: monolithic, DSSC, spacer layer, zirconia, thermal treatment, performance, sintering.

I. INTRODUCTION

At present, the silicon-based technology is the most popular product on the market and has achieved power conversion efficiencies of about 24%. The high production cost, the required of materials purity and sophisticated technological processes have prompted the researchers to find a solution to develop a new material for solar cells. Technology in the field of solar cells is becoming increasingly attractive since Professor Grätzel made a breakthrough in 1991 with the development of dye-based solar cells (DSSC). With power conversion efficiency up to 11.2%, this cell has been expected to be a potential candidate of the next generation solar cells [1], [2]. The technology offers several advantages such as low production cost, design opportunities, flexibility, lightweight, feedstock availability, better light harvesting in low and/or diffuse lighting, and with the possibility of higher cell stability due to simpler sealing [3], [4]. Although the efficiency of DSSC is still lower than that of silicon solar cells, research on DSSC is still having an opportunity to improve efficiency. These reasons make the DSSC an attractive renewable energy source for the future.

A typical DSSC is a sandwich structure based on two Fluorine-doped Tin Oxide (FTO) glass substrates. One FTO glass acts as a working electrode (anode) consisting of the nanocrystalline TiO_2 semiconductor layer,–which is sensitized to an inorganic dye. Another FTO glass was coated with platinum which serves as a counter electrode (cathode) [5]. Between these two substrates, I^-/I_3^- ionic liquid electrolyte is added which helps to reduce the oxidized dye [6].

The FTO glass substrate in the sandwich structure contributed almost 80% of the overall fabrication cost [7]. Therefore, some research is done to reduce the cost of DSSC fabrication. One of them is by developing DSSC with a monolithic structure, where the DSSC fabrication process is done in a single FTO glass substrate [7]. This structure offers the prospect of lower material cost and requires a simpler manufacturing process compared with sandwich structure [8], [9].

In monolithic structure, the working electrode and counter electrode are fabricated in a single FTO glass substrate with a planar-connected. A ZrO_2 layer is added between working electrode and counter electrode to prevent contact between the two electrodes. It also serves as electrolytes storage [7]-[9]. A carbon layer is used for counter electrode, replacing expensive platinum to realize further cost reductions. Figure 1 shows the comparison between the configuration structures of sandwich and monolithic DSSC.

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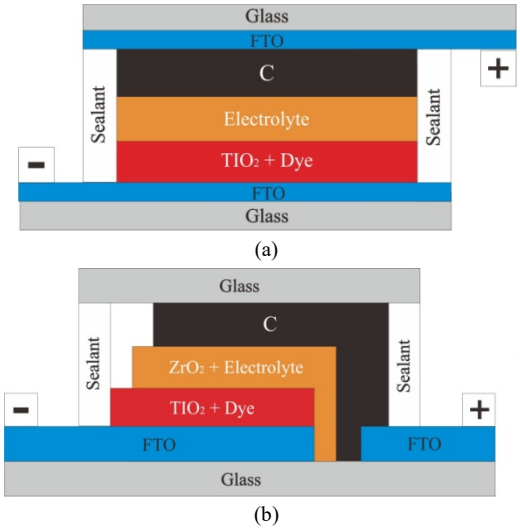


Figure 1. The Structure of DSSC (a) Sandwich and (b) Monolithic.

Although quite promising, the efficiency of DSSC monolithic is about 7.6%, lower than that of DSSC sandwich [10]. The low efficiency is caused by the higher series resistance of carbon or graphite layers being used, approximately twice the resistance of the FTO glass used. As the graphite is being used as the charge collector on the counter electrode, the series resistance of the cell will be increased [4]. Therefore, the research on monolithic DSSC is still wide open to obtain optimal performance. The previous study reported that the thickness of both spacer and counter-electrode materials have significant effects on the performance of monolithic DSSC [11].

The spacer layer on the monolithic DSSC has a function as transportation of electrolyte to dyed porous TiO_2 layer and a function as a spacing insulator to separate dyed TiO_2 layer and carbon layer electrically. The spacer layer is usually composed of a porous purely ZrO_2, Al_2O_3, or rutile-TiO_2 [9]. Zirconia (ZrO_2) is often used as a spacer because it has high temperature resistant, high dielectric constant and band gap 5-6 eV [12].

L. Vence *et al*. has done research by preparing a low-cost zirconia paste deposited via blade coating [6]. Zirconia thickness is determined by varying the height of the blade. As a transportation layer of electrolyte to dyed porous TiO_2 layer, the zirconia layer must have a small specific surface area and big pores size to avoid dye absorption and to favor the electrolyte percolation [6]. The porosity and particle size of the zirconia layer is also affected by thermal treatment. The present work focuses on the zirconia spacer layer, in particular, the role of the thermal treatment. The zirconia layer was deposited by the screen printing method. The layers were sintering at different temperatures in order to produce different porosity. The effects of the sintering temperature of the zirconia layer on the performance of monolithic DSSC have been investigated.

II. METHODOLOGY

A. Materials

Materials used in this research were obtained from various manufacturers. Fluorine-doped transparent oxide (SnO_2:F) coated glasses or FTO with a conductivity of ~15 Ω/sq (TEC15), TiO_2 paste (18NR-AO), dye-based ruthenium Z907, I^-/I_3^- ionic liquid electrolyte (EL-HPE), low temperature thermoplastic sealant (surlyn50), and sealing paste (Hermetic Sealing Compound) were purchased from Dyesol™, Australia. Meanwhile, the ZrO_2 paste (Zr-Nanoxide ZR/SP) was supplied by Solaronix, Switzerland. Carbon nanopowder and α-terpineol were supplied by Aldrich, Germany. Colloidal graphite was purchased from Polaron Instruments Inc. Acetone, ethanol, and ethyl cellulose were obtained from Merck, Germany. TiO_2 powder (P25) was purchased from Degussa, Germany. Isopropyl alcohol (IPA) was supplied by PT. Brataco, Indonesia.

B. Cell Fabrication

Figure 2 shows top view of the monolithic DSSC configuration design. The dimension of FTO substrate glass was 20 x 15 mm^2. The devices were fabricated by several steps. First, FTO with the area of 2 x 15 mm^2 was removed from the FTO glass substrate using sandpaper to separate the designated anode and cathode side. The glass substrates were then cleaned by ultrasonic cleaner bath (Branson 3200, Emerson Electric Co., USA) in acetone, detergent, deionized (DI) water, and isopropyl alcohol (IPA), for 10 min, respectively. After being dried, TiO_2 paste was printed on the conductive side of the FTO glass using de Haart SP SA 40 screen printer. The printing area was 7 × 10 mm^2. The deposition was carried out in two cycles, wherein the layer was dried in an oven at 120 °C for 10 min after each cycle. The layers were subsequently sintering at 500° C for 40 min in a conveyer belt furnace (Radiant Technology Corp., USA). The sintered layers were then immersed in 40 mM of $TiCl_4$ aqueous solution at 70 °C for 30 min and sintered again at 500° C for 40 min to obtain the TiO_2 reflector layer and to increase the surface area of the TiO_2 layer. So it will be able to improve the absorption of the dye and implies the optimization of the light harvesting [13].

Next steps, spacer layer ZrO_2 paste, was screen printed on top of the TiO_2 layer with an area of 7 × 7 mm^2. The deposition was carried out in two cycles and dried in an oven at 120 °C for 10 min in each cycle. After that, the layers sintered at various temperatures of 300 °C, 400 °C, 500 °C and 600 °C for 40 min for sintering treatment. For co-sintering treatment, the sintering was done after the deposition of the carbon counter electrode. A. S. Keiteb *et al*. reported that the zirconia calcination was done in the range of 600 – 900 °C [14]. According to this report, we decided to choose a maximum sintering temperature of 600 °C considering to the glass transition of the substrate.

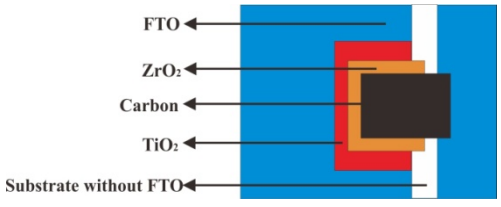


Figure 2. Top View of Configuration Design of Monolithic DSSC.

The carbon layer as a counter electrode was subsequently deposited on top of the ZrO_2 with a size of 8 × 5 mm^2. The layer was made by screen printed of carbon paste and dried in a conveyor oven at 120 °C for 20 min and then sintered at 400 °C for 30 min.

All samples were subsequently immersed in Z907 dye solution with a concentration of 0.25 mM for 24 hours in dark condition, to sensitize the TiO_2 particles. After they are dried in the air, the samples were covered with a glass slide and assembled using surlyn thermoplastic and pressed and heated at 120 °C for 30 seconds. Liquid electrolyte containing I^{3-}/I^- redox mediators was injected in the gap between the glasses, and finally, the gap was sealed with a hermetic compound. The complete monolithic DSSC fabrication process is presented in Figure 3.

C. Characterization

The crystal structure of the zirconia layers films was analyzed using X-ray diffraction (XRD) on Shimadzu Maxima XRD-7000 with Fe Kα source at λ=1.94 Å. The surface morphology was observed by JEOL JB-4610F field emission scanning electron microscopy (FESEM).

From the FESEM images, we also manually measured the particle size using Corel Draw Program. By measuring the length of the particles and the length of the scale as shown on the FESEM image, the particle size then can be determined by calculating the ratio of the length of the particles and the length of the scale with the size of the scale.

The photovoltaic properties of the cells were analyzed by measuring the current-voltage characteristics using National Instrument I-V measurement system, under xenon simulated solar (occupied with AM 1.5G filter) irradiation of 50 mW/m^2, at 25 °C. The active area of each cell was defined to be 2.5 x 10^{-5} m^2. The flowchart diagram of the monolithic DSSC fabrication process is expressed in Figure 3.

III. Results and Discussion

The photographs of the cells before assembly (a) and after the sealing process (b) are shown in Figure 4.

Figure 5 shows the XRD patterns of the ZrO_2 layer at different sintering temperatures. The patterns show the planes of (100), (011), $(11\bar{1})$, (111), $(21\bar{1})$, (022), (220), (202), (013), $(3\bar{0}2)$, and (311), which are corresponding to monoclinic ZrO_2 crystal phase according to JCPDS 37-1484 [15]. The purity of the monoclinic phase of ZrO_2 can be determined from the integrated intensities of the diffraction peaks $(11\bar{1})$ and (111) at $2\theta = 28.5^o$ and 31.5^o [16], [17].

The intensity of diffraction peaks increases with increasing of sintering temperature, which is indicating a significant enhancement in crystallinity.

The average crystallite sizes of the ZrO_2 can be calculated from the $(11\bar{1})$ diffraction peak. The crystallite size was determined from the full width at half maximum (FWHM) of the XRD patterns using the Scherer formula shown in (1):

$$D = \frac{0.9\,\lambda}{\beta \cos\theta} \quad (1)$$

where D is the crystallite size (nm), β is the full width of the diffraction line at half the maximum intensity measured in radians, λ is the X-ray wavelength of Fe Kα=0.194 nm and θ is the Bragg angle [14].

The calculations of the crystallite size of zirconia layers in different sintering temperature are presented in Table 1. It was found in the table that the crystallite size tends to increase at sintering temperature 300 °C to 400 °C. Then stable at 400 °C, 500 °C, and 600 °C. Based on this result, it is observed that the crystallite size is stable after sintering at 400 °C.

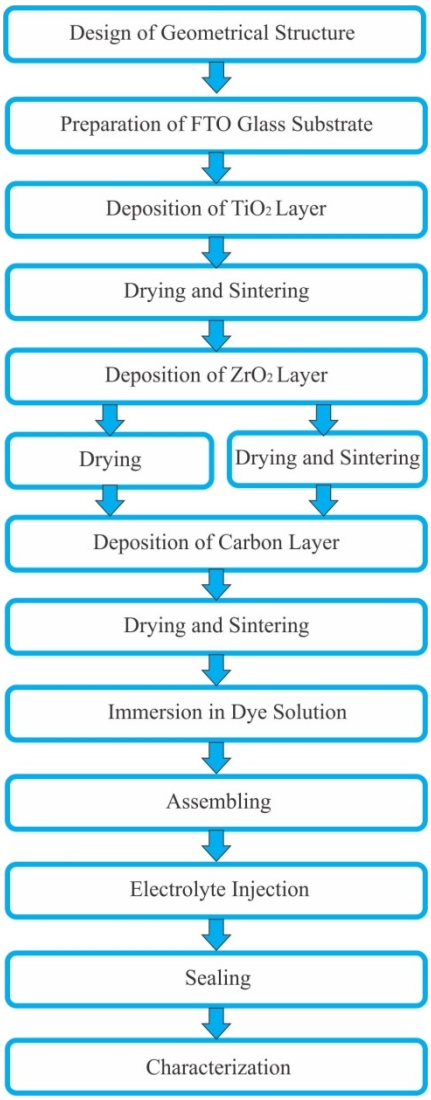
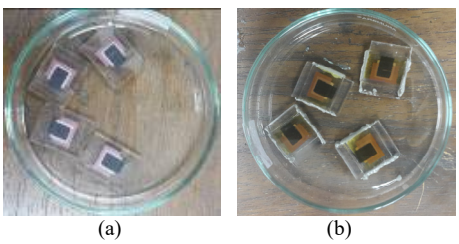


Figure 3. Flowchart Diagram of Monolithic DSSC Fabrication Process.



(a) (b)

Figure 4. Photographs of Monolithic DSSC (a) Before Assembly and (b) After Sealing

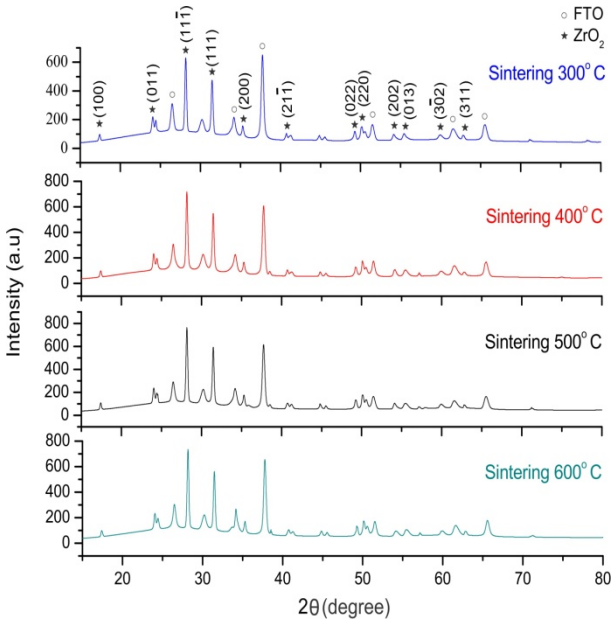


Figure 5. XRD Patterns of ZrO_2 Layer in Different Sintering Temperature.

TABLE 1
AVERAGE CRYSTALLITE SIZE CALCULATED FROM XRD PATTERNS

Sintering Temperature (°C)	Average Crystallite Size D_{XRD} (nm)
300° C	42
400° C	45
500° C	45
600° C	44

TABLE 2
RESULT MEASUREMENT OF ZIRCONIA PARTICLES SIZE

Sintering Temperature (°C)	Particles Size (µm)
300	0.14 – 0.85
400	0.13 – 1.26
500	0.12 – 0.40
600	0.12 - 1.26

The surface morphology of the zirconia layer was observed using FESEM images as shown in Figure 6. It can be seen from the figure that the surface morphology of the zirconia layer formed valleys (darker areas) at each sintering temperature, indicating the presence of pores or gaps between particles. From the figure, we can measure the particles size of the zirconia layer, and the results can be seen in Table 2. The particle size tends to decrease as the sintering temperature increases. This result is in accordance with the expectation, the smaller particle size, the more pores are formed, and the more the electrolyte can be diffused [18]. However, the increase of sintering temperature also increases the formation of big size pores or holes. The presence of big size pores or holes will allow the dye to pass through the zirconia layer and be absorbed into the TiO_2 layer [6].

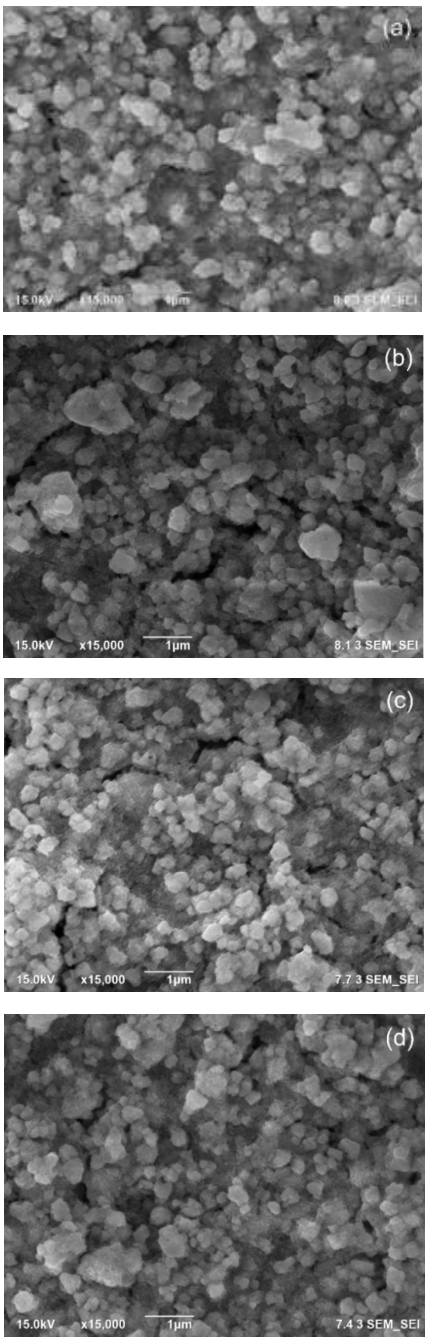


Figure 6. FESEM Images of Zirconia Layers in Different Sintering Temperature of (a) 300 °C (b) 400 °C (c) 500 °C (d) 600 °C.

Based on Table 1 and Table 2, it is observed that with the increase of sintering temperature of the zirconia layer, the crystallite size tend to stable, whereas the particle size is decreased. In addition, the size of the particle of the zirconia layer is about 3X larger than the crystallite size. A possible explanation is that the crystallite size is determined only from the highest peak of XRD pattern, thus representing only one crystal plane $(11\bar{1})$ (monocrystalline). In the particle structures, there are several crystals that formed by different planes (multi-crystalline); as shown in the XRD pattern, so that the particles size becomes larger compared to the lower temperature treatment.

The performance of a monolithic DSSC can be determined by measuring the I-V curve characteristic of current and voltage measurements. From the I-V curve,

a maximum power (P_{max}), a short-circuit current (I_{sc}), and an open-circuit voltage (V_{oc}) can be obtained. Fill factor (FF), and power conversion efficiency (PCE) can be calculated according to (2) and (3):

$$FF = \frac{V_{max} I_{max}}{V_{oc} I_{sc}} \quad (2)$$

$$PCE = \frac{P_{max}}{P_{in}} \, x \, 100\ \% \quad (3)$$

Where V_m, I_m, P_{in} are the maximum voltage, the maximum current, the power received from the incident illumination, which is dependent on the irradiation intensity and the active area of the cell [19].

I-V characteristics and electrical performance of the cells in different sintering and co-sintering temperature are shown in Figure 7 and Table 3. The results show that V_{oc} and I_{sc} increase with the increasing sintering temperature. Increasing in I_{sc} resulted in increased of P_{max} and the power conversion efficiency. Sintering at 500 °C and 600 °C gives similar results, but at sintering 600 °C there was a slight decrease in performance compared to sintering 500 °C. This may be due to structural phase changes in the zirconia layer at high temperatures. L. Vesce *et al*. has been investigated the effect of the ZrO_2 spacer film thickness on PV parameters [6]. They noticed that a J_{sc}, V_{oc}, FF, and PCE increase until to the optimal thickness of 11.5–15 μm. The thickness of the zirconia layer sintered at 500 °C (measured by cross-section view of FESEM image) is only 9.75 μm, which is thinner compared to Vesce et al. reported. S.J. Thompson *et al*. has been investigated a zirconia spacer layer with a thickness of 6 μm [4]. The differences of the optimum thickness could be due to the different zirconia paste which is used. However, the best results are obtained by sintering at 500 °C which produces V_{oc} = 0.71 V, I_{sc} = 0.16 mA, and PCE = 0.22%.

TABLE 3
PHOTOVOLTAIC PARAMETER MONOLITHIC DSSC VARIATIONS IN TEMPERATURE SINTERING AND CO-SINTERING OF ZIRCONIA

ZrO_2 Thermal Treatment	P_{max} (mW)	I_{SC} (mA)	V_{OC} (V)	FF	PCE (%)
Sintering 300 °C	0.01	0.03	0.14	0.30	0.01
Sintering 400 °C	0.02	0.08	0.61	0.28	0.11
Sintering 500 °C	0.03	0.16	0.71	0.24	0.22
Sintering 600 °C	0.03	0.14	0.71	0.26	0.21
Co-sintering 300 °C	0.01	0.06	0.55	0.29	0.08
Co-sintering 400° C	0.02	0.11	0.56	0.26	0.12
Co-sintering 500 °C	0.01	0.07	0.65	0.21	0.08
Co-sintering 600 °C	0.005	0.04	0.44	0.26	0.03

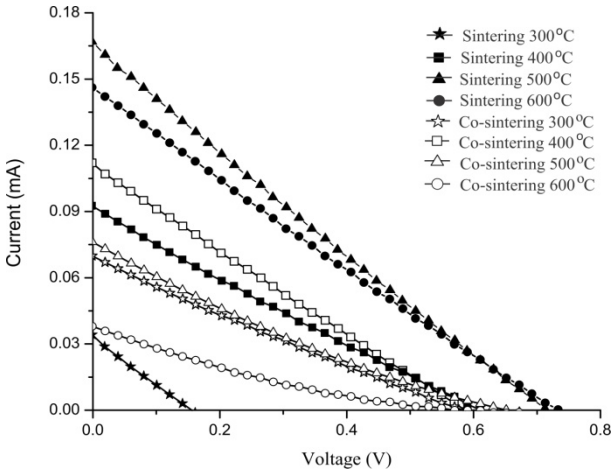


Figure 7. Current-Voltage (I-V) Curve of Monolithic DSSC at Different Sintering and Co-sintering Temperatures.

Co-sintering treatment tends to drastically reduce cell's performance, especially at a temperature level above 400 °C. It could be due to sintering above 400 °C undergo further crystallization and shrinkage of carbon layer [6]. As a result, the catalytic process of electrolyte (reduction of tri-iodide to iodide) in order to regenerate the oxidized dye reduced [9]. In addition, co-sintering above 400 °C also causes a reduction in the thickness of the carbon layer, resulting in low conductivity. As a consequence, the resistance and the charge generation and electron transfer become less, and the performance of the cells decreases.

CONCLUSION

The effects of the thermal treatment of the zirconia layer as a spacer electrolyte on the performance of monolithic DSSC have been investigated. The cell's performance increases with the sintering temperature of the zirconia layer as well as indicated by the decrease in particle size. Co-sintering treatment of zirconia layer and carbon layer tends to reduce cell's performance drastically. The best performance of monolithic DSSC was obtained at a zirconia sintering of 500° C with a PCE of 0.22%, I_{sc} = 0.16 mA and V_{oc} = 0.71 V.

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