Jurnal Elektronika dan Telekomunikasi (JET), Vol. 23, No. 2, December 2023, pp. 108-114
Accredited by KEMDIKBUDRISTEK, Decree No: **158/E/KPT/2021**
doi: 10.55981/jet.563

Design of Brushless DC Motor Driver Based on Bootstrap Circuit

Khoirudin Fathoni*, Esa Apriaskar, Nur Azis Salim, Vera Noviana Sulistyawan, Rifki Lukman Satria, Syahroni Hidayat

Department of Electrical Engineering
Universitas Negeri Semarang
Sekaran, Gunungpati
Semarang, Indonesia

Abstract

A brushless DC (BLDC) motor is a three-phase that requires electronic commutation to replace the brush function in the DC motor. This paper aims to implement BLDC motor driver integration based on bootstrap circuits using Autodesk Eagle. The study proposes an emphasis on bootstrap capacitor calculation based on the charging/discharging capacitor principle with motor speed rotation as well as the pulse width modulation (PWM) frequency and duty cycle. The driver board consists of a bootstrap circuit based on IR2110, MOSFETs, three voltage regulators, ESP32 microcontroller and ACS712 current sensor connection, logic level converter, and BLDC hall effect signal sensor conditioning. The implemented driver has a 14 ×10 cm dimension tested to drive 24 V/135 W/6000 rpm sensored BLDC motor using six steps commutation with PWM inserted programmatically in ESP 32 to drive the high side MOSFET of the driver without AND gate circuit. The effect of PWM frequency and duty cycle variation on the speed and current of the motor is investigated. The results showed that the driver with both 12 V and 24 V voltage source and 68 µF bootstrap capacitor work optimally in 20 kHz PWM frequency both in open loop and closed loop speed control tests. The motor reaches 129 W for the largest power and 5250 rpm for the fastest speed in a 24 V supply.

Keywords: BLDC motor, 3 phases motor driver, bootstrap circuit.

I. Introduction

A brushless DC (BLDC) motor is a type of magnet permanent motor with electronic commutation instead of brush like in a brushed dc motor. Although called a DC motor, a BLDC motor is a three-phase motor that cannot work directly with DC current but requires electronic commutation to replace the brush function in a DC motor [1]. In the absence of a brush, the BLDC motor has advantages such as less maintenance for brush replacement, bigger torque, better dynamic performance, and higher efficiency [2]. So that the BLDC motor has become more popular and used in various fields as a drive system for automotive, robotics, aviation, the factory, and household appliances [3], [4]. Nevertheless, since the BLDC motor requires electronic commutation, it needs a more complex driver than a DC motor.

BLDC motor needs 3 phase voltage source inverter based on electronics switching components like MOSFETs or IGBTs, and they must conduct properly to give appropriate current to drive the motor [5]. Ready-to-use BLDC drivers are already available on the market. However, each switching component in the driver cannot be accessed individually to achieve better performance with advanced control such as vector control [6], [7] and model predictive control [8], [9]. Moreover, custom drivers will be more suitable for specific motors.

The challenging factor in BLDC motor driver design is each phase consists of high-side and low-side switching devices. The high-side source is floating and needs voltage reference to reach gate-to-source threshold voltage, which results in the high side conducting the current. Two popular methods to design high-low side drivers are based on optocoupler and bootstrap circuits. TLP250 is often used in optocoupler-based drivers [10], [11]. This method provides good isolation for low and high voltage [12]. However, this circuit requires four independent voltage sources with different ground [13]. In addition, it has a lower switching frequency than the bootstrap-based circuit. Meanwhile, the bootstrap circuit provides faster switching with only one ground. Either IR2101 [14] or IR2110 [15] bootstrap IC has been used in the design. IR2110 has the advantage since it provides a separate logic supply [16].

In [17], [18] designed and simulated IR2106 and IR2101-based drivers in Proteus software, respectively. In [19], the IR2110-based driver was built for 350 W BLDC with a 5 V microcontroller and hall effect sensor signal conditioning, while [20] was built for 1 kW BLDC without signal conditioning. Since the driver in previous research is based on 5 V, potential improvement can be achieved to get lower power consumption and faster control based on a 3.3 V microcontroller. Moreover, in [20], hall effect sensors have not been utilized for speed sensor yet, while [19] and [15] only use one sensor for speed reading that will give limitation especially in BLDC with few magnet pairs. In addition, one of the

* Corresponding Author.
Email: khoirudinfathoni@mail.unnes.ac.id
Received: August 01, 2023 ; Revised: October 30, 2023
Accepted: November 06, 2023 ; Published: December 31, 2023

most important steps in the IR2110 BLDC driver, that is, to get the appropriate value of the bootstrap capacitor, needed to be explained. To control BLDC speed, current to the motor can be regulated by the PWM technique. Because PWM frequency and duty cycle that regulate current have time duration for high and low states, they can affect bootstrap capacitor condition and should be considered.

This paper aims to explain the design and implementation of the BLDC motor driver using the IR2110 bootstrap circuit. In addition, an electronic circuit for voltage regulator, hall effect sensors signal conditioning, ESP32 3.3V microcontroller modules, as well as two ACS712 current sensor modules, all integrated on a single PCB. The study to find bootstrap capacitors is important because inappropriate values can cause driver failure. Moreover, the single custom driver implemented is useful to get a compact BLDC driver motor that can be controlled by either PWM or direct control technique. This study contributes to build a BLDC driver by bootstrap circuit with detailed analysis in getting bootstrap capacitor from capacitor charge/ discharge based on speed and PWM frequency and duty cycle. The driver will have superiority in compactness due to single board integration, with appropriate bootstrap capacitor value to drive the BLDC motor properly.

The rest of the paper is organized as follows. Section II explains the driver design for each block. Section III describes the results of driver implementation and analyzes its performance, and section IV gives the conclusion.

II. METHOD

The block diagram of the BLDC motor drive is illustrated in Figure 1. Two poles pair sensored BLDC motor with three hall effect sensors is used. The signals of three hall effect sensors are utilized for commutation and speed sensors. A 24 V supply is the main source of the power of the BLDC motor, and then it is stepped down into 15 V, 5 V, and 3.3 V. A 15 V for IR2110 VCC, 5 V for hall sensor effect and ESP32 input power supply, while 3.3 V for logic supply Vdd of IR2110, 74HC14, and 74HC86.

A logic level converter is needed to change 5 V hall effect sensor outputs to 3.3 V. Then, the 3.3 V output of hall effect sensors is connected to the 74HC14 inverting Schmitt trigger. Outputs of the 74HC14 are connected to the ESP32 board as digital input pins for commutation as well as to the 74HC86 XOR gate. The signal from the XOR gate is then connected to ESP32 as an interrupt pin to determine the ellapse time for speed calculation. Six digital output pins of ESP32 are connected to the high and low side input of IR2110 (HIN and LIN) to control the switching component, which usually consists of IGBT or MOSFET. The IGBT is preferred in high-voltage and high-power applications, while MOSFET is selected for faster switching frequency [21].

MOSFET is used instead of IGBT in this driver because BLDC is low-power and can still be handled by MOSFET, and higher-frequency BLDC motor control can be accommodated. Space for two current sensors based on ACS712 20 A is provided in the PCB. The

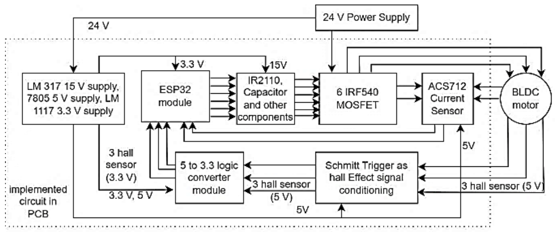

Figure 1. Block diagram of BLDC motor driver design

ACS712 works with a 5 V supply and results in the analog voltage directly proportional to BLDC current [22] to measure rms current [23]. The voltage divider circuit using two series resistors in series is used to get 0 - 3.3 V range output of the current sensor from 0 - 5 V range. The integrated PCB is designed using Autodesk Eagle.

A. Voltage regulator and logic converter circuit

A 24 V supply is regulated into 15 V using an LM317 circuit, which is shown in Figure 2. The maximum tolerable input voltage is 40 V. The 15 V VOUT is obtained from a proper combination of R17 and R18 by (1) [24]. IADJ is very small so can be neglected. So, if R18=3.3 kΩ, R17 should be 36.3 kΩ. A variable resistor is used for R17 to tune the value to get 15 V output.

$$V_o = 1.25\left(1+\frac{R_{17}}{R_{18}}\right)+\left(I_{ADJ}\times R_{17}\right) \tag{1}$$

15 V from LM317 is regulated into 5 V and 3.3V by using L7805 and AMS1117 3.3 V, respectively. The logic level converter circuit module is used to change the 5 V hall effect sensor output voltage to 3.3V. The module and its schematic can be seen in Figure 3. HV and LV are 5 V and 3.3 V, respectively. Only three pairs of logic converters are used from the four available in the module.

B. IR2110 and MOSFETs circuit

The next block is the IR2110 MOSFET driver. The bootstrap circuit principle mainly consists of the charging and discharging process of the capacitor. The schematic of the bootstrap circuit-based on IR2110 and MOSFET circuit for one phase is shown in Figure 4. The supply VCC of IR2110 is taken from LM317 output and the VDD from AMS1117 for 3.3 V with C5, C6 for 15 V voltage stabilization, and C1, C2 for 3.3 V voltage stabilization. HIN and LIN are connected to ESP32 digital output to control the high and low side MOSFET, respectively. Logic ‘1’ for HIN will correspond to turn

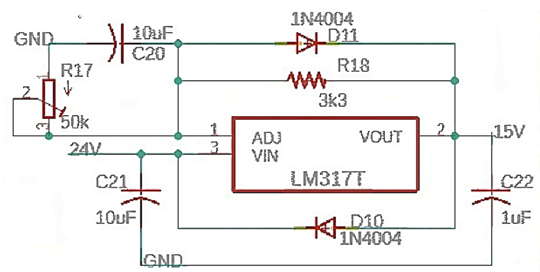

Figure 2. LM317 voltage regulator circuit

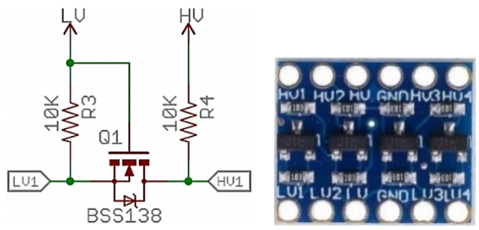

Figure 3. 5 volt to 3.3 logic converter circuit

on the high MOSFET (Q1) through HO, while logic '1' for LIN will turn on the low MOSFET (Q4) through LO.

However, high MOSFET cannot turn on with logic '1' to HIN because IR2110 works with bootstrap principal through bootstrap capacitor C3. Small C4 (ceramic capacitor) is required in parallel with C3 to give a small ESR, if the C3 is an electrolytic capacitor [25].

Q1 and Q4 MOSFET must not be in conduction mode (ON) at the same time. When LIN=1, LO will give VGS for Q4 so that the low MOSFET will conduct and bootstrap capacitor C3 is in charging condition. Current flow from VCC passes UF4007 fast recovery, switching diode to C3, then to VS1 (V phase 1), Q4, and GND (black flow) when LO OFF an HO ON, bootstrap capacitor C3 will discharge (yellow flow) so they act like a voltage source and give reference voltage for floating VS1 as a source of Q1. Current will flow to VB, HO, and give VGS for Q1 so that Q1 will conduct. Bootstrap C3 should charge quickly while LO is in ON condition. Nevertheless, they must have enough voltage to give reference voltage for VGS of Q1 during HO at ON condition.

The value of C_3 can be determined in [26] by only charging/ discharging capacitor analysis without considering other aspects. However, this value is a minimum value, and motor speed still needs to be considered to find the value so that the capacitor is too small and will discharge quickly even though Q1 MOSFET should still be conducting. This condition will lead to high-side driver failure because VGS is not enough to turn on the high-side Q1 MOSFET, so the motor fails to rotate. So, it is concluded that the faster the motor speed, the smaller capacitor is enough. On the other hand, for slower rotation, a bigger value of the capacitor is needed to achieve the VGS threshold. This research proposes a C3 value based on a one-revolution-per-second (rps) motor speed condition. For a two-pole

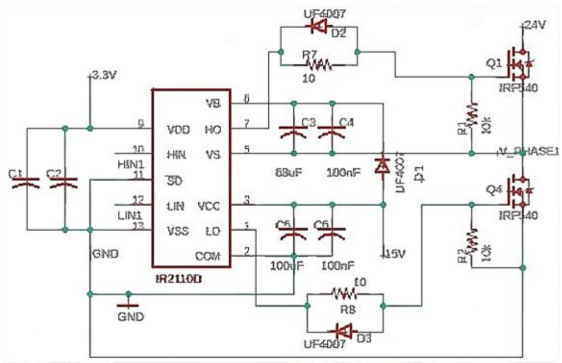

Figure 4. IR2110 and MOSFET circuit with bootstrap flow operation for one phase

pair of BLDC motors there will be 12 commutations with 4-time sequences for each phase to achieve 1 rps. Therefore, it needs 0.25 seconds to charge and discharge the bootstrap (C3) capacitor in a cycle. The C_3 can be analyzed by the discharge capacitor equation through R1. Based on (2), C3 should be > 47 μF to get only a 0.7 V discharge drop of the capacitor into 13 V, which is higher than minimum gate drive voltage (12 V) and fully drive the MOSFET. A 13.7 V is obtained by 98% of IR2110 VCC (capacitor voltage in settling time condition) that is subtracted with UF4007 forward voltage (1 V).

$$13 = 13.7\, e^{\frac{0.25}{10^5 C_3}}$$
$$C_3 = 4.77 \times 10^{-5} \cong 47\mu F \tag{2}$$

If 68 μF is chosen in this design, the remaining capacitor voltage from (3) after the next 0.25 s is 13.2 V. So, the voltage drops during bootstrap capacitor discharging at 1 rps speed is only 0.5 V. When the bootstrap C3 is in discharging state, the capacitor will discharge through R1 = 100 kΩ series and Rgate (R7) =10 Ω (can be ignored).

$$V_{C_3} = 13.7\, e^{-\frac{0.25}{10^5 \times 68 \times 10^{-6}}} = 13.2\, V \tag{3}$$

The required settling time (T_s) of 98% to achieve 12 V from 0 V can be calculated by (4). The resistance element of the charging loop, which consists of the internal resistance of Rds-on of IRF540 MOSFET, is 0.055 Ω. To gets 12 V for minimum VGS voltage, the required time charge of 98% is 5.47 μs.

$$12 = 15\left(1 - e^{-\frac{T_s}{0.055 \times 68 \times 10^{-6}}}\right)$$
$$T_s \cong 5.47\, \mu s \tag{4}$$

This Ts is required at the beginning of driver operation to charge the bootstrap capacitor from 0 to 13.7 V. But, when the motor has rotated at 1 rps so that the bootstrap capacitor voltage drops based on (3) only 0.5 V, the charging time required to achieve 13.7 V from 13.2 V is only 1.6 μs. Based on (4), the maximum PWM frequency can be known. Nevertheless, the frequency should not be too high to get a linear and wider range of speed and does not exceed MOSFET's maximum switching frequency. Besides the rotational speed of the motor, the effect of PWM frequency and duty cycle on the capacitor value can be considered, which is calculated in (5) with the capacitor charging process in the startup condition with a 10% duty cycle. A 10 % duty cycle in 20 kHz PWM frequency will have a 5 μs bootstrap charging time.

$$12 = 15\left(1 - e^{-\frac{5\mu s}{0.055 \times C_3}}\right)$$
$$C_3 = 5.64 \times 10^{-5} \cong 56\, \mu F \tag{5}$$

The value is still between 47 μF and 68 μF, so the driver will work properly in this PWM frequency. On the other hand, when a much higher frequency is applied to the driver, for instance, 100 kHz with a 10% duty cycle will have only 1 μs to charge C_3. By using (5), the C_3 will be only 11 μF. This value is too small below 47 uF (2) so that when C3 is in discharge condition while high side

MOSFET is ON, the capacitor voltage will decrease quickly below minimum gate voltage.

C. Hall Effect Sensor Signal Conditioning

Schmitt trigger-based conditioning signal is used to generate almost ideal hall effect sensor signal output pulses. Noisy, fluctuated, and unsharpened hall effect sensor signals lead to rotor position misreading. Double inverting Schmitt trigger 74HC14 is used and implemented on a 3.3 V supply.

The inputs are taken from 3.3 V hall effect sensor signals after being converted from 5 V by a logic level converter. Three output signals of 74HC14 are combined to produce a tighter pulse signal for the speed sensor by the 74HC86 XOR gate. The schematic is shown in Figure 5.

III. Results and Discussion

The implementation of the driver connected to the BLDC is shown in Figure 6, which has 14 cm × 10 cm in dimension. The driver was tested to drive 24 V/ 135 W/ 6000 rpm, two magnet pairs, sensored BLDC motor with six step commutation method. To determine the correct phase sequence of the BLDC, an experiment was carried out by giving voltages combination to the three BLDC phases and viewing the output from the hall effect sensor to obtain Table 1.

Phase voltage and hall effect sensors are codded with their cable colour. The ESP32 microcontroller board is programmed to run the six commutations with two active conduction phases based on the hall effect sensor condition to rotate BLDC in a clockwise direction without load.

To rotate clockwise, the digital pin of ESP32 must read the hall effect sensor condition. When the sensor is 101, the motor is given a -++ voltage, 001 is given -+- and so on. Furthermore, PWM generated from ESP32 is applied to the active high side of MOSFET through the HIN pin of IR2110 when the bootstrap circuit is in discharge condition so that it does not disturb the charging process. Then, the program reads the ACS712 current sensor through the Analog to Digital Converter (ADC) pin. For the speed measurement, the output of the XOR gate is connected to the ESP32 external interrupt pin. The driver was tested by a 24 V supply and a 12 V supply to give a more comprehensive result in voltage variation effect and correlation to the driver.

The results of the experiment can be seen in Table 2 and Table 3 for 12 V and 24 V supply voltage,

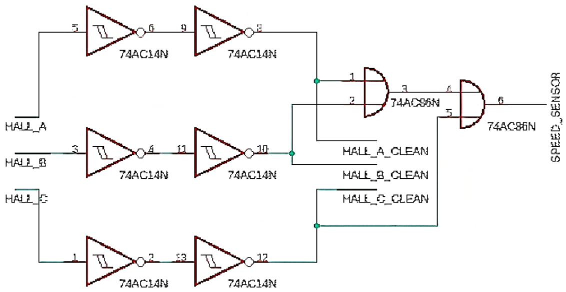

Figure 5. Schmitt trigger and XOR gate for hall effect signal conditioning circuit

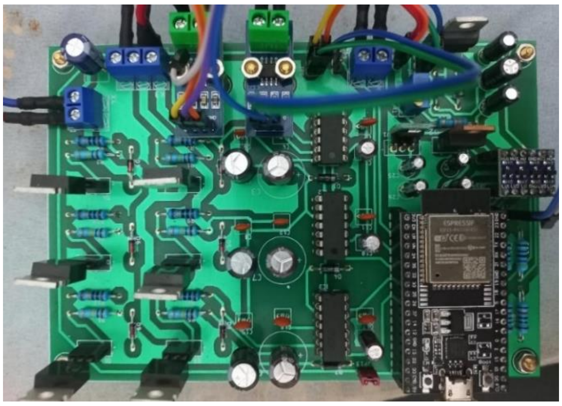

Figure 6. BLDC motor driver implementation.

respectively. The effect of changes in the PWM duty cycle, PWM frequency and voltage supply to speed and RMS current of BLDC motor measured by ACS712 sensor were observed as well. The driver was tested with three variations of the PWM frequency, 5 kHz, 20 kHz, and 100 kHz.

The result shows that PWM frequency affected the range and linearity of the duty cycle to the BLDC speed. 10% duty cycle for 12 V in 5 kHz can rotate the motor; but in contrast, for 100 kHz with the same duty cycle (10%), the motor was not rotating. Moreover, audible noise is present at 5 kHz for all duty cycle values because this frequency is in the range of audio frequency, while in two higher frequencies, both in 20 kHz and 100 kHz, these noises disappear.

The correlation of PWM frequency to speed linearity is investigated using linear regression shown in Figures 7 and 8. PWM to speed correlation should be linear to achieve better control system performance. The speed linearity of 24 V decreased compared to 12 V, especially in high duty cycle in the range 90% to 100% for all frequencies. The speed was saturated because the motor reached maximum speed and voltage.

For the 12 V supply, the data indicates that for both 5 kHz and 20 kHz frequencies in the 10% duty cycle, the motor rotated because the ON duty cycle is on 20 µs and 5 µs, respectively, with speed for 5 kHz frequency in 30%-60% duty cycles tend to faster than the speed both in 20 kHz and 100 kHz. However, the 5 kHz frequency had a bigger current ripple and nonlinearity since the current dropped drastically during the OFF-cycle condition.

On the other hand, 100 kHz frequency or 10 µs PWM period, 10% ON duty cycle happened 3 µs less than Ts, it was insufficient to charge C3 as bootstrap capacitor as in (4). The duty cycle was too small to charge the bootstrap capacitor and turn on the high MOSFET on the

TABLE 1
PHASE VOLTAGE TO HALL EFFECT SENSOR CONDITION

Phase Voltage			Hall sensor condition		
Red	Yellow	Green	Blue	White	Green
+	-	+	1	0	1
-	-	+	0	0	1
-	+	+	0	1	1
-	+	-	0	1	0
+	+	-	1	1	0
+	-	-	1	0	0

TABLE 2
BLDC DRIVER OBSERVATION IN 12 V

Duty cycle (%)	**5 kHz**		**20 kHz**		**100 kHz**	
	rad/s	I(A)	rad/s	I(A)	rad/s	I(A)
0	0	0	0	0	0	0
10	11	0.05	10	0.04	0	0.01
20	57	0.2	46	0.08	45	0.07
30	111	0.35	83	0.16	81	0.14
40	155	0.43	120	0.23	121	0.22
50	194	0.48	159	0.32	159	0.31
60	228	0.45	200	0.41	194	0.39
70	254	0.54	238	0.54	234	0.51
80	285	0.7	278	0.67	272	0.67
90	313	0.88	315	0.79	312	0.8
100	350	0.9	351	0.89	350	0.89

next cycle. This is in accordance with calculation (4): if the period is less than T_s, the bootstrap C3 is not charged enough while the low MOSFET is ON to reach minimum V_{GS}, so that when the high MOSFET is ON, not enough V_{GS} voltage to drive the MOSFET.

In addition, in 100 kHz PWM frequency, the current does not have enough time during ON condition to reach the motor winding and achieve the motor electrical time constant. This led to the presence of current, although the motor was not rotating. It also shows that 20 kHz and 100 kHz show a similar pattern except for a 10% duty cycle in 12 V, in which the motor was not rotating at 100 kHz. This led to the best linearity in 20 kHz.

In comparison, for the 24 V supply, the non-zero duty cycle starting from 5% was enough to rotate the motor. The motor was rotating from a 5%-100% duty cycle for all frequencies with different behavior. The speed for 5 kHz frequency in 20 % - 70 % duty cycles was faster than the speed both in 20 kHz and 100 kHz with a nonlinear curve. So, in terms of speed linearity to the duty cycle, 5 kHz exhibits the worst linearity among two others in both 12 V and 24 V, indicated by the lowest R^2 value and 20 kHz linearity achieve the greatest value.

Power delivery performances over duty cycle alteration shown by current behavior are displayed in Figure 9 and Figure 10 with linear regression for both 12 V and 24 V supply voltage, respectively. The 5 kHz shows the biggest average RMS current, although it tends to be nonlinear as the duty cycle increases. Meanwhile,

TABLE 3
BLDC DRIVER OBSERVATION IN 24 V

Duty cycle (%)	**5 kHz**		**20 kHz**		**100 kHz**	
	rad/s	I(A)	rad/s	I(A)	rad/s	I(A)
0	0	0	0	0	0	0
5	9	0.17	9	0.19	9	0.13
10	54	0.52	41	0.5	41	0.3
20	166	1.15	107	0.7	107	0.62
30	267	1.55	176	1.18	175	1.14
40	366	1.96	246	1.54	246	1.49
50	417	2.13	321	1.93	322	1.9
60	470	2.24	393	2.44	393	2.4
70	513	2.78	448	2.99	449	2.84
80	523	3.4	515	3.62	512	3.45
90	525	4.9	525	4.77	523	4.76
100	550	5.38	550	5.37	547	5.36

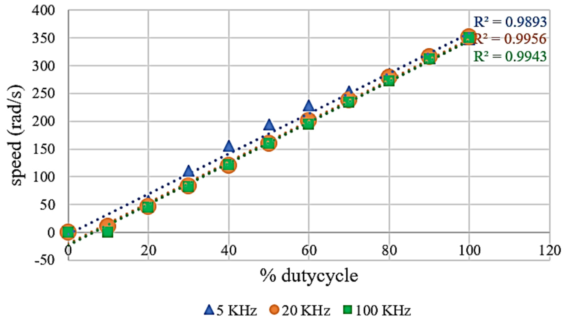

Figure 7. Duty cycle to speed linearity in 12 V.

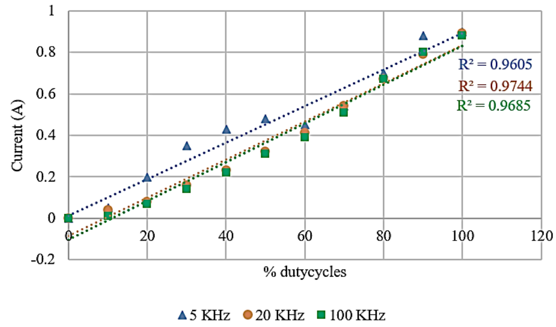

Figure 8. Duty cycle to speed linearity in 24 V.

100 kHz exhibits the lowest power because of the low average RMS current. This low current is caused by switching losses in fast PWM frequency, while 20 kHz has the highest current linearity with moderate current. The power comparison between 24 V and 12 V is that of course 24 V has larger power than 12 V because 24 V supply has a bigger current, but the current exhibits different behavior. The linearity of current over duty cycle in 24 V declines compared to 12 V 20 kHz is the most linear, and 5 kHz is the lowest.

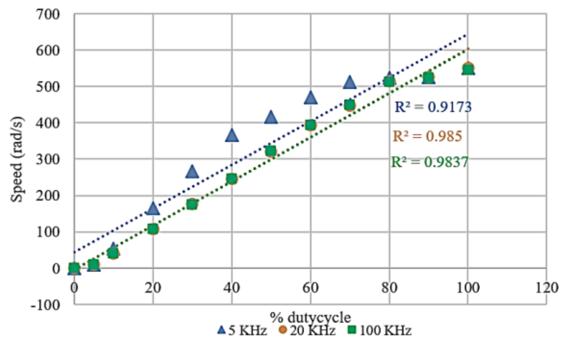

Figure 9. Duty cycle to current linearity in 12 V.

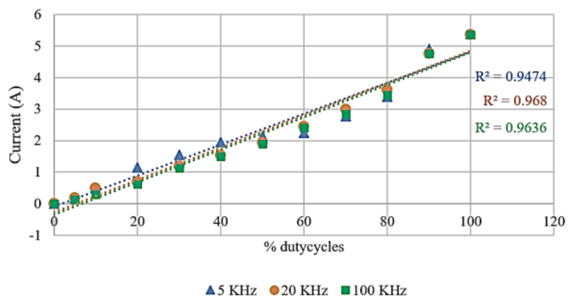

Figure 10. Duty cycle to current linearity in 24 V.

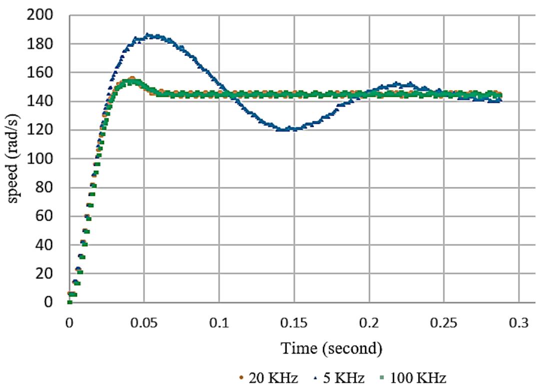

Figure 11. Closed loop control step response

The motor open loop performance using the driver in a 12 V supply can achieve 10 W with a speed of 350 rad/s or 3342 rpm, and the largest power, 129 W, is achieved in a 24 V supply with 550 rad/s or 5250 rpm while both supply in full duty cycle and almost same current value for all frequencies in respective supply voltage.

Besides open-loop performance, the driver is also examined by closed-loop control using simple Proportional Integral Derivative (PID) control to find out the effect of PWM frequency for closed-loop speed control. Digital PID based on backward difference approximation was implemented in ESP32 [27]. Uniform PID parameters (K_p, K_i, K_d) by manual tunning with 100 µs time sampling and constant set point speed are used to test three PWM frequency variations like the open loop test. The step responses of the speed with 150 rad/s set point in 12 V supply are shown in Figure 11 with the summary of time response parameter in Table 4.

Based on the system response, it is noticeable that PWM frequency influenced the control system performance of the BLDC motor. The results are different when using the same control method and time sampling. The 5 kHz frequency had the worst performance in terms of peak time, overshoot, settling time, and steady-state error, with only the fastest on-rise time. The better performance was achieved by 20 kHz and 100 kHz with similar characteristics. However, 100 kHz had 0.002 s dead time at the beginning of its response. So, it results in a slightly slower rise, peak and settling time compared to 20 kHz.

Compared to previous research, many of them are directly focused on control system performance. In [15], the IR2110 bootstrap circuit is implemented, but the study is focused on the fuzzy logic control performance of BLDC. The study in [20] also used an IR2110-based driver, which was tested to drive 48 V/ 1 kW BLDC. It reached 278 W with a 48 V supply using a 94 % PWM duty cycle.

The driver implemented on [19] achieves 111.2 W to drive 350 W BLDC motor in 90 % duty cycle with 48 V supply while this study in the same duty cycle can reach 114 W of 135 W BLDC motor. However, the driver closed-loop performance and PWM frequency variation were not explored. Furthermore, the PWM signal as gate driver from the microcontroller was delivered through AND gate, which added component and complexity in the circuits as well as time delay to send the PWM signal from the microcontroller to the gate driver. Moreover, the driver, microcontroller, and other modules in [15] and [20] were still separated. In addition, the bootstrap circuit and capacitor value design in [15], [19] and [20] are not investigated in detail. In contrast, the PWM frequency inserted in the driver plays an important role in the motor performance both in open loop and close loop control systems.

TABLE 4
CLOSED LOOP PERFORMANCE COMPARISON

Parameter	5 kHz	20 kHz	100 kHz
Rise time (s)	0.023	0.025	0.027
Peak time (s)	0.054	0.041	0.043
% Overshoot	24	1.5	1.4
Settling time (s)	0.2	0.046	0.047
Steady state error (%)	0.05	0.02	0.02

IV. CONCLUSION

In summary, this study has implemented a compact single-board BLDC motor driver based on the bootstrap circuit with detailed bootstrap capacitor calculation based on capacitor charge/discharge based on speed as well as PWM frequency and duty cycle. The driver was tested to drive a 24 V/ 135 W/ 6000 rpm sensored BLDC motor. To control the current delivered to the motor, PWM was inserted with duty cycles and frequency variation was investigated to find the correlation and its effect on the driver and motor performance.

Experimental results confirm that 20 kHz PWM frequency achieved the best performance compared to 5 kHz and 100 kHz in terms of duty cycle to current and speed linearity and closed loop speed control performance in step response setpoint including rise time, peak time, % overshoot, settling time, and steady-state error using PID controller. The motor open loop performance using the driver reached the largest power, 129 W in 24 V supply with r 5250 rpm. This driver with 20 kHz PWM frequency can be used to control BLDC motors with more advanced methods in the future.

DECLARATIONS

Conflict of Interest

The authors have declared that no competing interests exist.

CRediT Authorship Contribution

Khoirudin Fathoni: Conceptualization, Methodology, Investigation, Software, Formal Analysis, Validation, Data Curation, Writing-Original Draft; Esa Apriaskar: Methodology, Data Curation, Investigation, Writing-Reviewing & Editing; Nur Azis Salim: Resources, Data Curation; Vera Noviana Sulistyawan: Visualization, Resources, Project administration; Rifki Lukman Satria: Resource, Data Curation, Investigation; Syahroni Hidayat: Supervision, Validation, Writing-Reviewing & Editing.

Funding

Research reported in this publication was supported by Universitas Negeri Semarang under grant number: DIPA-023.17.2.677507/2022 under 2022 Basic Research Scheme of Engineering Faculty of UNNES Number: 28.13.4/UN37/PPK.4.5/2022.

Acknowledgment

The authors would like to thanks to Education Laboratory Staff of Electrical Engineering Department, Universitas Negeri Semarang for supporting and preparing the equipment, electronic components, and instrumentations required for experimental study.

REFERENCES

[1] A. S. Al-Adsani, M. E. AlSharidah, and O. Beik, "BLDC motor drives: a single hall sensor method and a 160° commutation strategy," *IEEE Trans. Energy Convers.*, vol. 36, no. 3, pp. 2025–2035, Sep. 2021, doi: 10.1109/TEC.2020.3046183.

[2] S. Derammelaere, M. Haemers, J. De Viaene, F. Verbelen, and K. Stockman, "A quantitative comparison between bldc, pmsm, brushed dc and stepping motor technologies," in *19th Int. Conf. Electr. Mach. Syst. (ICEMS)*, Nov. 2016, pp. 1-5. [Online]. Available: https://ieeexplore.ieee.org/document/7837471

[3] D. Mohanraj *et al.*, "A review of bldc motor: state of art, advanced control techniques, and applications," *IEEE Access*, vol. 10, pp. 54833–54869, 2022, doi: 10.1109/ACCESS.2022.3175011.

[4] B. Banu Rekha, B. Somasundaram, L. Ashok Kumar, and P. Balekai, "A technical review on advantages of using ec bldc fans in factory and commercial buildings," *Energy Eng.*, vol. 115, no. 3, pp. 57–74, May 2018, doi: 10.1080/01998595.2018.12002418.

[5] K. FATHONI and A. B. UTOMO, "Perancangan kendali optimal pada motor arus searah tanpa sikat melalui metode lqri," (in Indonesia), *ELKOMIKA J. Tek. Energi Elektr. Tek. Telekomun. Tek. Elektron.*, vol. 7, no. 2, p. 377, May 2019, doi: 10.26760/elkomika.v7i2.377.

[6] K. C. N. Sridivya and T. V. Kiran, "Space vector pwm control of bldc motor," in *2017 Int. Conf. Power Embed. Drive Control*, Mar. 2017, pp. 71–78. doi: 10.1109/ICPEDC.2017.8081062.

[7] Z. Li, J. Wang, L. Zhou, X. Liu, and F. Jiang, "Enhanced generalized vector control strategy for torque ripple mitigation of ipm-type brushless dc motors," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12038–12049, Dec. 2019, doi: 10.1109/TPEL.2019.2906247.

[8] A. G. de Castro, W. C. A. Pereira, T. E. P. de Almeida, C. M. R. de Oliveira, J. Roberto Boffino de Almeida Monteiro, and A. A. de Oliveira, "Improved finite control-set model-based direct power control of bldc motor with reduced torque ripple," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4476–4484, Sep. 2018, doi: 10.1109/TIA.2018.2835394.

[9] M. S. Trivedi and R. K. Keshri, "Evaluation of predictive current control techniques for pm bldc motor in stationary plane," *IEEE Access*, vol. 8, pp. 46217–46228, 2020, doi: 10.1109/ACCESS.2020.2978695.

[10] K. V. K. Varma and A. Ramkumar, "Implementation of spv-powered water pumping system using non-isolated sc converter topology," *Electr. Eng.*, vol. 103, no. 3, pp. 1433–1444, Jun. 2021, doi: 10.1007/s00202-020-01170-9.

[11] S. Kıvrak, T. Özer, and Y. Oğuz, "Design and implementation of dspic33fj32mc204 microcontroller–based asynchronous motor voltage/frequency speed control circuit for the ventilation systems of vehicles," *Meas. Control*, vol. 52, no. 7–8, pp. 1039–1047, Sep. 2019, doi: 10.1177/0020294019858097.

[12] O. A. Qudsi and S. D. Nugraha, "Desain dan implementasi pengaturan kecepatan motor bldc melalui pengaturan fluks," (in Indonesian), *INOVTEK - Seri Elektro*, vol. 1, no. 1, p. 36, Dec. 2019, doi: 10.35314/ise.v1i1.1231.

[13] K. Fathoni, "Perancangan dan implementasi sistem kendali kecepatan motor magnet permanen tiga fasa sebagai motor arus searah tanpa sikat," Institut Teknologi Bandung, 2014.

[14] Z. Syroka, "A controller for brushless direct current electric motors. part 1. electrical and electronic design," *Tech. Sci.*, vol. 23, no. 2020, pp. 185–198, Dec. 2020, doi: 10.31648/ts.5695.

[15] M. Wirandi, Safril, F. Sumasto, M. Agus, and F. Imansuri, "BLDC motor design by applying the control of direct current and analysis of loading mechanism soft starting," *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 885, no. 1, p. 012005, Jul. 2020, doi: 10.1088/1757-899X/885/1/012005.

[16] International Rectifier, "Datasheet ir2110(s)pbf/ir2113(s)pbf high and low side driver," 2019. [Online]. Available: https://www.infineon.com/cms/en/product/power/gate-driver-ics/ir2110/

[17] A. Stevanus, Y. Calvinus, and D. Santun Naga, "Simulation of brushless dc motor controller in sem electric car prototypes," *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 1007, no. 1, p. 012177, Dec. 2020, doi: 10.1088/1757-899X/1007/1/012177.

[18] M. F. Bhuiyan, M. Rejwan Uddin, Z. Tasneem, M. Hasan, and K. M. Salim, "Design, code generation and simulation of a bldc motor controller usuuing pic microcontroller," in *2018 Int. Conf. Recent Innov. Electr. Electron. Commun. Eng.*, Jul. 2018, pp. 1427–1431. doi: 10.1109/ICRIEECE44171.2018.9008910.

[19] F. Rohman, N. Nurhadi, G. Gumono, M. E. Martawati, M. Z. Fanani, and D. S. Hormansyah, "Design and implementation of a 350-watt bldc motor driver using an insulated gate bipolar transistor (igbt)," *IOP Conf. Ser. Mater. Sci. Eng.*, vol. 732, no. 1, p. 012097, Jan. 2020, doi: 10.1088/1757-899X/732/1/012097.

[20] P. Astuti and H. Masdi, "Sistem kendali kecepatan motor bldc menggunakan pwm berbasis mikrokontroler arduino uno," (in Indonesian), *JTEIN J. Tek. Elektro Indones.*, vol. 3, no. 1, pp. 120–135, Jan. 2022, doi: 10.24036/jtein.v3i1.216.

[21] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance evaluation of high-power sic mosfet modules in comparison to si igbt modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181–1196, Feb. 2019, doi: 10.1109/TPEL.2018.2834345.

[22] T.-Y. Ho, F.-T. Liu, G.-W. Ho, and Y.-R. Lin, "The implementation of a measurement system for brushless dc motor parameters," *Int. J. Green Energy*, vol. 14, no. 12, pp. 983–995, Sep. 2017, doi: 10.1080/15435075.2017.1350184.

[23] Đ. Lazarević, M. Živković, Đ. Kocić, and J. Ćirić, "The utilizing hall effect-based current sensor acs712 for true rms current measurement in power electronic systems," *Sci. Tech. Rev.*, vol. 72, no. 1, pp. 27–32, 2022, doi: 10.5937/str2201027L.

[24] M. Pauzan and I. Yanti, "Penggunaan pin adc (analog to digital converter) pada mikrokontroler atmega8535 untuk menghasilkan catu daya digital," (in Indonesian) *ELKHA J. Tek. Elektro Untan*, vol. 11, no. 2, pp. 122–127, 2019, doi: http://dx.doi.org/10.26418/elkha.v11i2.35036.

[25] H. Wang, C. Li, G. Zhu, Y. Liu, and H. Wang, "Model-based design and optimization of hybrid dc-link capacitor banks," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8910–8925, Sep. 2020, doi: 10.1109/TPEL.2020.2971830.

[26] Y. Lee and J. Kim, "Analysis of bootstrap circuit operation with an inverted pwm drive scheme for a three-phase inverter for a brushless dc motor drive," *Can. J. Electr. Comput. Eng.*, vol. 42, no. 1, pp. 58–65, 2019, doi: 10.1109/CJECE.2019.2891850.

[27] F. ISDARYANI, M. F. V. HESYA, and F. FERIYONIKA, "Sintesis kendali pid digital dengan diskritisasi langsung dan backward difference," (in Indonesian), *ELKOMIKA J. Tek. Energi Elektr. Tek. Telekomun. Tek. Elektron.*, vol. 9, no. 2, p. 467, Apr. 2021, doi: 10.26760/elkomika.v9i2.467.