Jurnal Elektronika dan Telekomunikasi (JET), Vol. 23, No. 2, December 2023, pp. 85-90
Accredited by RISTEKDIKTI, Decree No: **158/E/KPT/2021**
doi: 10.55981/jet.558

Estimating the Differential Mode Noise of Basic DC-DC Converters

Yoppy[a,*], Dwi Mandaris[a], Aditia Nur Bakti[a], Hutomo Wahyu Nugroho[a],Yudhistira Yudhistira[a], Deny Hamdani[b]

[a]Research Center for Testing Technology and Standards
National Research and Innovation Agency
Building 417, B.J. Habibie Technopark,
South Tangerang, Indonesia
[b]Research Center for New and Renewable Energy,
School of Electrical and Informatics Engineering, Institut Teknologi Bandung,
Jalan Ganesha 10, Labtek VIII Lantai 2, Bandung,
Jawa Barat, Indonesia

Abstract

Electromagnetic noise emission is inevitable in a DC-DC converter due to the employed switching technique. In low frequency, the noise propagating through cabling and conductive media is called a conducted emission. A conducted emission consists of differential mode and common mode noise. It is advantageous to know an estimate of the emission level for each mode during the design phase so that suitable mitigation can be included earlier. This paper aims to focus on a method to estimate the differential mode noise emission of a DC-DC converter. The estimation is computed using the input capacitor complex impedance and the current that flows through it. As a study case, boost and buck converters are used for evaluation. The estimation and measurement results are compared. Despite differences at some frequencies, the estimated and measured results generally agree well. Because of its simplicity, the proposed method can be used as a practical tool in the EMC aspect of DC-DC converter design.

Keywords: buck converter, boost converter, complex impedance, differential mode noise, input capacitor

I. INTRODUCTION

Nearly every modern electronic device uses a DC-DC converter as its power supply because it is cost-effective, small, and highly efficient. However, DC-DC converters pose a major problem in terms of electromagnetic noise generation. At the heart of a DC-DC converter is a high frequency chopping of the power supply current, from tenths of kHz up to a few MHz. Consequently, undesirable electromagnetic noises are generated and propagated to the environment through conduction and radiation.

A conducted emission (CE) is made up of common mode (CM) and differential mode (DM) components. The CM component flows through capacitive coupling paths formed between the DC-DC converter and the environment, whereas the DM component flows. In contrast, the DM component flows through capacitive coupling paths formed between the DC-DC converter and the environment. In contrast, the DM component flows through the path where the main switching current travels. Because of their different propagation paths, CM and DM noise are suppressed with different filter configurations. In order to be effective in dimensioning a CM or DM noise filter, in practice, the CM/DM noise level is first measured on the converter board using a tool that can separate each of the noises [1]-[3] . The CM/DM noise separator works by adding/subtracting the CE on the positive and negative lines concurrently. Once the CM/DM noise level is obtained, the corresponding filters can be designed properly.

Furthermore, it would be very beneficial if the noise level could be predicted earlier through calculation rather than later through measurement. In that way, the noise level can be anticipated during the design process, allowing for earlier incorporation of the necessary measures. In [4]-[6], prediction is made to the CE as a whole by thoroughly modeling each component in the converter and put them all together in a circuit simulation. In [7] and [8], the prediction is focused on the CM noise of the component converter. This paper, focuses on the DM component and takes a simpler approach. The proposed DM noise estimation method does not require circuit simulations, and is based on the multiplication of input capacitor complex impedance and the current that flows through it. For comparison, capacitors with different complex impedances are employed. An off-the-shelf boost and buck converters are used as experimental examples. Finally, a comparison between the estimation and measurement results is presented.

* Corresponding Author.
Email: yoppy.chia@gmail.com
Received: June 27, 2023 ; Revised: August 13, 2023
Accepted: September 1, 2023 ; Published: December 31, 2023

II. Materials and Methods

A. DC-DC Converters

1) Boost Converter

The example boost converter is a non-synchronous one built using the controller XL6009. The input and output voltages are 7.4 V and 12 V, respectively. The boost converter is coupled to a 4W load and switched at 200kHz in continuous conduction mode (CCM). The power inductor of the converter is 33 µH. Figure 1 shows the photograph of the boost converter.

Figure 1. Photograph of the boost converter.

2) Buck Converter

A non-synchronous buck converter based on the XL4015 controller is used in the experiment. The input and output voltages are 8 V and 5 V, respectively. The buck converter is connected to a 4.7 Ω resistor and is switched at 180 kHz in CCM mode. The power inductor is 47 µH. Figure 2 shows the photograph of the buck converter.

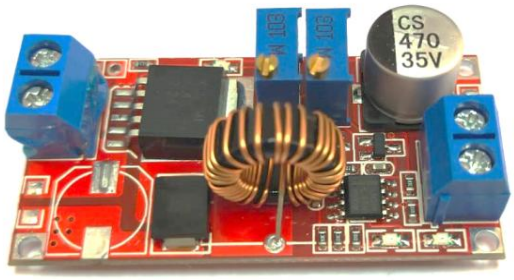


Figure 2. Photograph of the buck converter.

B. Input Capacitors

Due to the large amount of energy required at the input of a DC-DC converter, a high capacitance-voltage (CV) electrolytic capacitor is commonly used. There are three types of electrolytic capacitors: aluminum electrolytic capacitor, tantalum electrolytic capacitor, and niobium electrolytic capacitor. Owing to its price and performance advantages, aluminum electrolytic capacitor is the most popular in DC-DC converter applications. Aluminum electrolytic capacitors themselves are divided into two categories, i.e., liquid electrolytes and solid electrolytes. Due to the chemical properties, the latter is superior in terms of lower equivalent series resistance (ESR), which then results in lower complex impedance.

For comparison, three different input capacitors are used. Capacitors A, B, and C have the following ratings: 50 V, 100 µF; 50 V, 10 µF; and 100 V, 47 µF, respectively. Photographs of the capacitors are shown in Figure 3. Their complexiimpedances are measured using a vector network analyzer (E5071C) in the frequency range of 100 kHz up to 30 MHz. The magnitudes of the complex impedances are shown in Figure 4. Capacitor A is a liquid electrolytic capacitor, whereas Capacitor B and C, whose lower impedances are of solid electrolytic capacitors. The capacitors are installed alternately, and the DM noise of the converter is measured for each installed capacitor.

C. DM Noise Estimation Method

1) Boost Converter

Figure 5 shows a simplified schematic of a boost converter, where the input capacitor (C_{IN}) is represented by a voltage source (V_{CIN}) in series with a complex impedance (Z_{CIN}), where V_{CIN} and Z_{CIN} symbolize the capacitor charge voltage and the internal impedance, respectively. The impedance of an input capacitor is usually much lower than that of the power supply. It is clearly shown when the power supply wiring and LISN inductances are considered. Therefore, the fast switching current in the converter is primarily supplied by the input capacitor. In a steady-state condition, as illustrated in Figure 5, current that flows through the input capacitor (i_{CIN}) is an identical but DC-shifted version of the current flowing through the power inductor (i_L). DC current from the power supply is denoted by i_{PS}.

Assuming that C_{IN} capacitance is sufficiently large to keep V_{CIN} constant during switching, then V_{DM} is at a DC voltage superimposed with high frequency ripples due to a voltage drop at Z_{CIN}. This ripple voltage is essentially the DM noise. Thus, the proposed method of DM noise estimation $V_{DM_{BOOST}}$ is calculated as follows:

$$V_{DM_{BOOST}}(f) = Z_{CIN}(f) x i_{CIN}(f) \quad (1)$$

Figure 3. Photographs of capacitors A, B, and C.

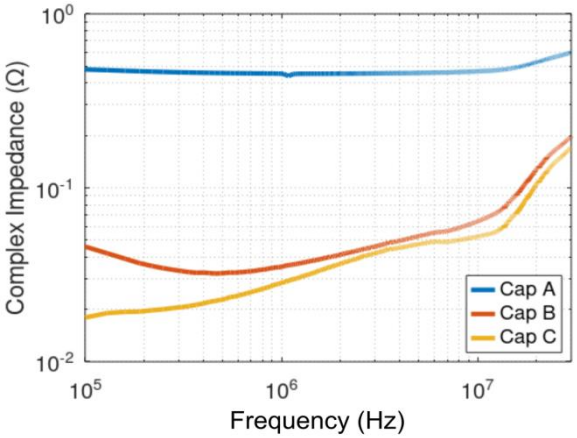


Figure 4. Complex impedance magnitude of input capacitors A, B, and C.

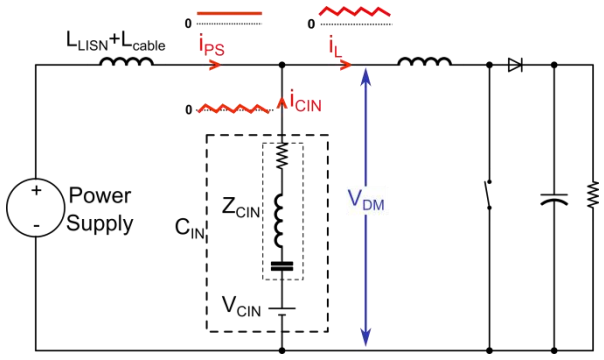


Figure 5. Simplified schematic of a boost converter.

where $Z_{CIN}(f)$ is the input capacitor complex impedance magnitude, $i_{CIN}(f)$ is the input capacitor current transformed into the frequency domain. Because it is element-wise multiplication, the frequency range and spacing of $Z_{CIN}(f)$ and $i_{CIN}(f)$ must be matched. Also, because i_{CIN} and i_L waveforms are basically identical, for convenient i_L waveform is used in place of i_{CIN}. The ac part of i_L waveform, as depicted in Figure 6, is constructed based on key parameters calculated from the following equations [9][10]:

$$\Delta I_L = \frac{VxD_{ON}}{f_S x L} \quad (2)$$

$$D_{ON} = \frac{V_{OUT}-V+V_D}{V_{OUT}+V_D} \quad (3)$$

In this paper, the waveform construction, frequency domain transformation, DM noise calculation, and plotting are all performed using Octave.

2) Buck Converter

Figure 7 shows the schematic of a buck converter, where the input capacitor (C_{IN}) is represented by a voltage source (V_{CIN}) in series with a complex impedance (Z_{CIN}). The input capacitor largely supplies high frequency switching current demanded by the converter. As illustrated in Figure 7, in a steady-state condition, the input capacitor current (i_{CIN}) waveform is identical but DC-shifted of the switch current (i_{SW}) waveform. Presume that the C_{IN} capacitance is large enough to maintain V_{CIN} constant during switching, then V_{DM} is at a DC voltage superimposed with high frequency ripples due to a voltage drop at Z_{CIN}. This ripple voltage is basically the DM noise, and therefore, the proposed method of DM noise ($V_{DM_{BUCK}}$ estimation is computed as follows:

$$V_{DM_{BUCK}}(f) = Z_{CIN}(f) x i_{CIN}(f) \quad (4)$$

where $Z_{CIN}(f)$ is the input capacitor complex impedance magnitude and $i_{CIN}(f)$ is the input capacitor current transformed into the frequency domain.

Due to the identicality of i_{SW} and i_{CIN} waveshape, for convenient i_{SW} is used in place of i_{CIN}. The i_{SW} waveform, as illustrated in Figure 8, is constructed according to principal values obtained from the following equations:

$$P_{OUT} = \frac{1}{2T}.L.{I_{L.AVG}}^2 \quad (5)$$

$$I_{SW.MID} = I_{L.AVG}\sqrt{\frac{P_{OUT}.2T}{L}} \quad (6)$$

$$\Delta I_{SW} = \frac{V-V_{OUT}}{L}.\frac{D_{ON}}{f_s} \quad (7)$$

$$I_{SW.PK} = I_{SW.MID} + \frac{\Delta I_{SW}}{2} \quad (8)$$

$$I_{SW.VAL} = I_{SW.MID} - \frac{\Delta I_{SW}}{2} \quad (9)$$

$$D_{ON} = \frac{V_{OUT}+V_D}{V+V_D} \quad (10)$$

The derivation of equation (5) – (10) is based on Figures 7 and 8 and is described as follows. During switch ON, the ramp-up switch current (i_{SW}) is equal to that of the inductor current (i_L). Therefore, $I_{SW.MID}$, which is the mid-value between $I_{SW.PK}$ and $I_{SW.VAL}$, is equal to the inductor average current $I_{L.AVG}$. The $I_{L.AVG}$ can be then deduced and calculated from the fact that energy stored in the inductor is for powering the output load, as described in Equations (5) and (6). Equation (7) is the basic formula for calculating the inductor current ramp-up when the switch is ON. From equation 6 and 7, the peak ($I_{SW.PK}$ and valley ($I_{SW.VAL}$ of the switch current can be obtained as in equations (8) and (9), respectively. After obtaining the value of D_{OFF}, D_{ON}, $I_{SW.PK}$, and $I_{SW.VAL}$, the waveform in Figure 8 can be constructed. In this paper, the waveform construction, frequency domain transformation, DM noise calculation, and plotting are carried out in Octave.

Note that the estimation method used in this paper

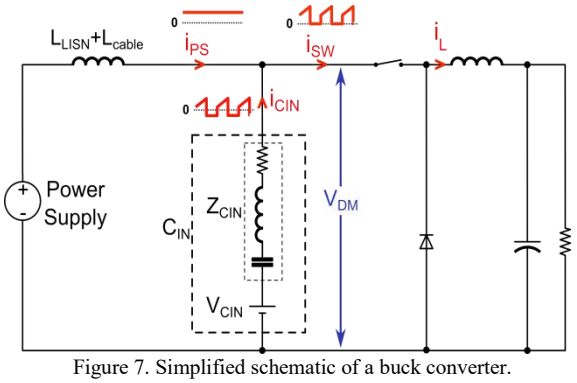


Figure 7. Simplified schematic of a buck converter.

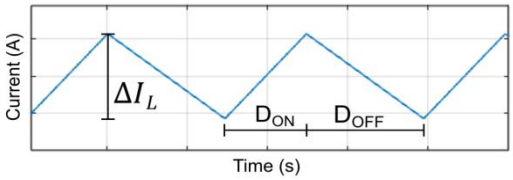


Figure 6. Conceptual inductor current (i_L) waveform.

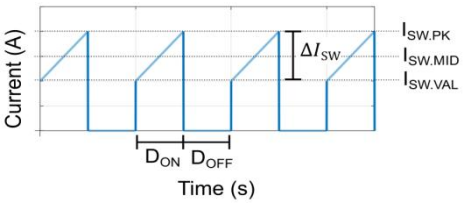


Figure 8. Conceptual switch current i_{sw} waveform.

is made simpler by excluding the effect of LISN, whereas in an actual measurement, a dual-LISN is connected to the converter's input (Figure 9). In general, LISN impedance is significantly larger than an input capacitor impedance. Take the LISNs used in this paper as an example. The dual-LISN DM impedance, which is twice the single LISN impedance, is around 6 Ω at 100 kHz and is rising to roughly 100 Ω at 5 MHz and onwards [11]. The LISN impedance is in parallel with the capacitor impedance, which effect,lowers the overall DM impedance at the converter's input. However, the difference is considerably small. The largest effect of LISN impedance would happen to capacitor A at low frequencies because, at low frequency, the difference between the capacitor impedance and LISN impedance is at a minimum. For example, near the switching frequency at 200 kHz, the impedance of capacitor A is 0.45 Ω, and the LISN DM impedance is 12 Ω. Then, the parallel impedances are equivalent to 0.433 Ω. In the logarithmic scale, the difference is 0.34 dB. Furthermore, lower discrepancies are expected at other frequency points and even lower for capacitors B and C.

D. DM Noise Measurement Method

For comparison with the estimation results, measurements of the DM noise are performed with a setup as shown in Figure 9. Two identical 5uH DC-LISNs are used [11] , and the converter input is connected to the LISNs. The LISN-MATE, which is a DM-CM separator, is used to measure the DM noise emission [12] purely . Internally in the LISN-MATE, DM noise at the DM output port is obtained by subtracting the conducted emission (CE) signal flowing in the positive and negative lines of the power supply. The unused CM output port is terminated with 50 ohm. The power supply, LISNs, LISN-MATE, and DC-DC converter are placed above a metallic ground plane. The spectrum analyzer is set to measure in peak detector mode.

III. Results and Discussions

A. Boost Converter

Figure 10 shows the DM noise comparison between the estimation and measurement results. In the case of capacitor A, good agreement between the estimation and measurement is shown in the whole frequency range. For capacitor B, the estimation is accurate from the fundamental frequency up to several harmonics and starts showing deviation from frequency above 2MHz. Meanwhile, for capacitor C, higher discrepancies are starting from the fundamental frequency and onwards. However, the general trends of the estimation and measurement results are matched quite well. Previously in [13], the DM noise estimation was done by considering only the capacitor series resistance (ESR). The complex impedance method used in this paper shows better accuracy.

As generally known in DC-DC converter design, converter's input/output is preferably coupled with a low impedance capacitor as it will result in lower ripples. From the EMC point of view, and as shown in Figure 10, low impedance capacitors result in low DM noise emission.

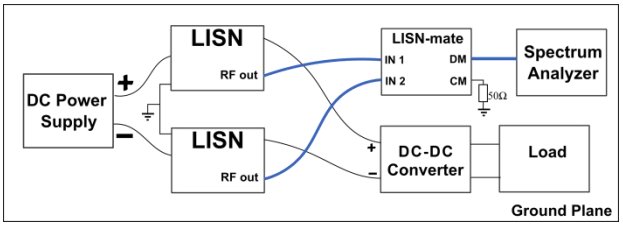
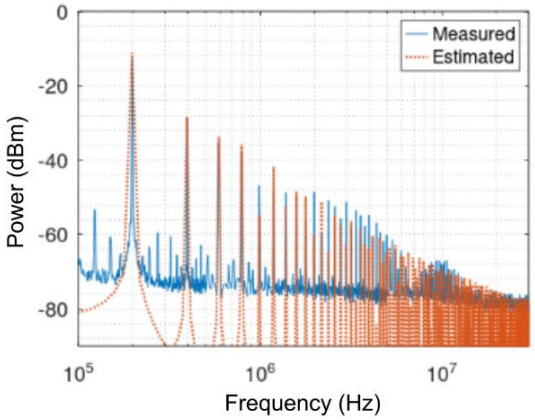
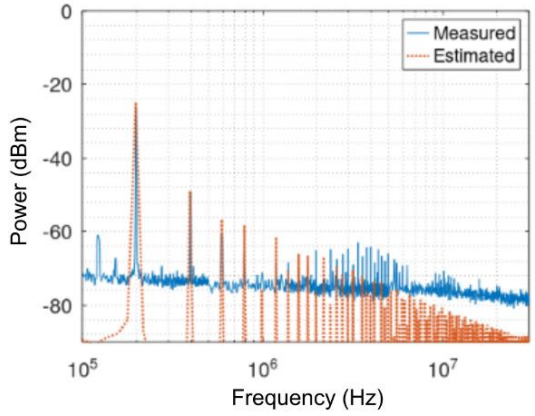


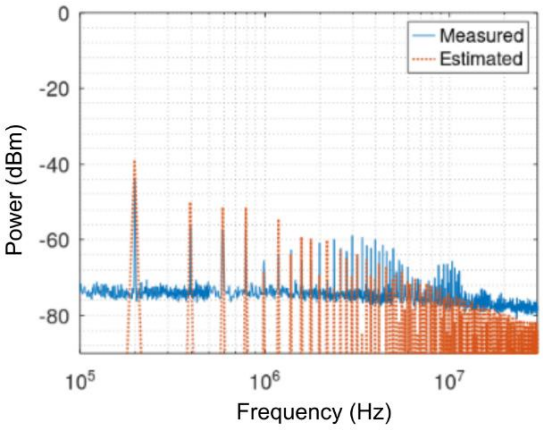
Figure 9. Setup of DM noise measurement.



(a) with input capacitor A



(b) with input capacitor B

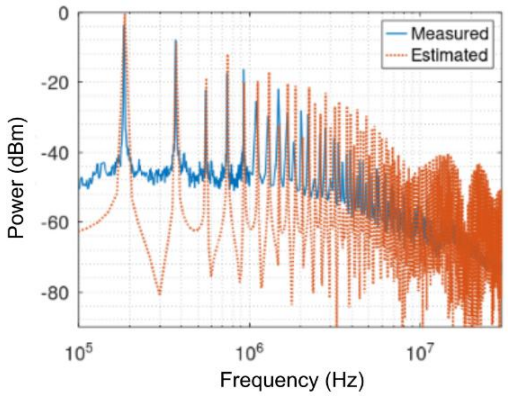


(c) with input capacitor C

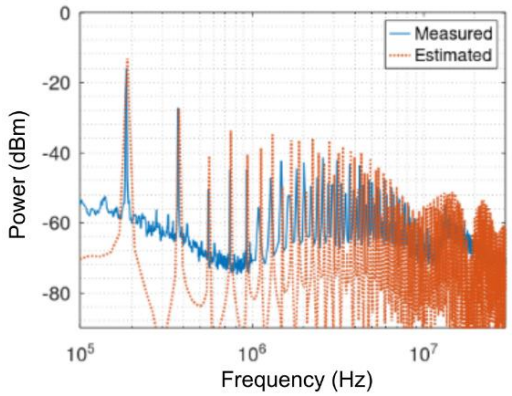
Figure 10. Comparison of DM noise estimation and measurement of the boost converter with input capacitors A, B, and C.

B. Buck Converter

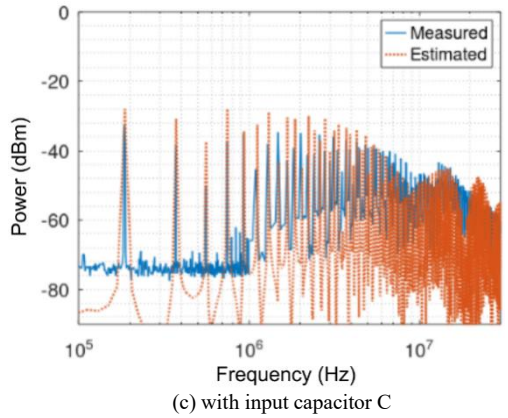
Figure 11 shows the comparison of DM noise estimation and measurements in a buck converter. In the estimation, the rising and falling edges of the waveform in Figure 8 are all set to 110 ns, as this number is approximate to the actual measurement. The steepness of rising and falling edges dictate the estimation accuracy in high frequency region starting from a few MHz and onwards. Therefore, due to the nature of a buck converter's input current waveshape, the rising and falling times should be roughly known to estimate the DM noise correctly in the high frequencies. As can be seen in Figure 11, there are some discrepancies in high frequency regions because the actual rising and falling times may deviate from the values fed in calculations. Nevertheless, the general trends of estimation and measurement are still in good agreement.



(a) with input capacitor A



(b) with input capacitor B



(c) with input capacitor C

Figure 11. Buck converter DM noise comparison with input capacitors A, B, and C.

IV. Conclusion

DM noise estimation based on the input capacitor complex impedance and the current flowing through it has been presented. A buck and boost converter are used for demonstration. The proposed method can serve as a practical tool in the EMC aspect of DC-DC converter design. Provided that the input capacitor complex impedance data are available, the DM noise emission can be estimated at design time. Therefore, suitable measures such as using lower impedance capacitors that meet the design requirements can be incorporated.

In addition, it is generally recommended that different types of capacitors, such as electrolytes and ceramics, can be combined to improve the filtering performance of input capacitors. This idea can be more systematically applied by exploiting the method proposed in this paper. Complex impedance of paralleled capacitors can be calculated from the known impedance of individual capacitors. Then, the DM noise level across a frequency range can be predicted. This result will give a more detailed picture of the expected EMC performance of such parallel capacitors.

Declarations

Conflict of Interest

The authors have declared that no competing interests exist.

CRediT Authorship Contribution

Yoppy: Methodology, Investigation, Writing-Original draft preparation; Dwi Mandaris: Writing-Reviewing and Editing, Supervision, Funding Acquisition; Aditia Nur Bakti: Writing-Reviewing and Editing; Hutomo Wahyu Nugroho: Writing-Reviewing and Editing; Yudhistira Yudhistira: Writing-Reviewing and Editing; Deny Hamdani: Writing-Reviewing and Editing, Funding Acquisition.

Funding

The research reported in this publication was supported by Institut Teknologi Bandung (ITB) and KEMENDIKBUDRISTEK under the grant of Applied Research Project, ANRGI 2022.

Acknowledgment

The authors would like to express gratitude to the Applied Electromagnetic Research Group at Research Center for Testing Technology and Standard – BRIN, Research Organization for Electronics and Informatics – BRIN, Research Center for New and Renewable Energy, School of Electrical and Informatics Engineering – ITB for the support and keen interest in promoting research and development by providing the facilities and time.

References

[1] S. Wang, F. C. Lee, and W. G. Odendaal, "Characterization, evaluation, and design of noise separator for conducted emi noise diagnosis," *IEEE Trans Power Electron*, 2005, doi: 10.1109/TPEL.2005.850978.

[2] C. R. Paul and K. B. Hardin, "Diagnosis and reduction of conducted noise emissions," *IEEE Trans Electromagn Compat*, 1988, doi: 10.1109/15.8769.

[3] T. Guo, D. Y. Chen, and F. C. Lee, "Separation of the common-mode- and differential-mode-conducted emi noise," *IEEE Trans Power Electron*, 1996, doi: 10.1109/63.491642.

[4] A. Boyer, M. A. G. Sentis, C. Ghfiri and A. Durier, "Modeling methodology of the conducted emission of a DC-DC converter board," *2017 11th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMCCompo)*, St. Petersburg, Russia, 2017, pp. 73-78, doi: 10.1109/EMCCompo.2017.7998085.

[5] A. Hamouda, Z. Riah, F. Ndagijimana and S. Serpaud, "Development of Electronic Board Conducted Emissions Model EBEM-CE using the bottom-up approach," *2014 International Symposium on Electromagnetic Compatibility*, Gothenburg, Sweden, 2014, pp. 751-755, doi: 10.1109/EMCEurope.2014.6931004.

[6] A. Durier, C. Marot and O. Crepel, "Using the EM simulation tools to predict the Conducted Emissions level of a DC/DC boost converter: Introducing EBEM-CE model," *2013 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, Nara, Japan, 2013, pp. 152-157, doi: 10.1109/EMCCompo.2013.6735191.

[7] P. Kong, Y. Jiang, and F. C. Lee, "Common mode emi noise characteristics of low-power ac-dc converters," *IEEE Trans Power Electron*, 2012, doi: 10.1109/TPEL.2011.2162100.

[8] S. Zhang, B. Zhang, and M. Shoyama, "Modeling and prediction of common-mode conducted noise in boost converter with terminal port theory," *10th International Conference on Power Electronics - ECCE Asia*, 2019. doi: 10.23919/icpe2019-ecceasia42246.2019.8797342.

[9] E. Rogers, "Understanding boost power stages in switchmode power suppliies," Texas Instruments Application Report, 1999.

[10] J. Hubner, "Power supply design tutorial (part 1-2) – topologies and fundamentals," (2018). Accessed : Mar. 10, 2023. [Online]. Available : https://www.powerelectronicsnews.com/power-supply-design-tutorial-part-1-2-topologies-and-fundamentals-continued/

[11] Mayerhofer. *TBL0550-1 5µh line impedance stabilisation network manual.* (2021). Accessed: June 26,2023. [Online]. Available : https://www.tekbox.com/product/TBL0550-1_Manual.pdf

[12] Mayerhofer. *TBLM1 lisn-mate user manual*. (2020). Accessed : June 26, 2023. [Online]. Available : https://www.tekbox.com/product/TBLM1_LISN_Mate_Manual.pdf.

[13] Yoppy, D. Mandaris, A. N. Bakti, H. W. Nugroho, Y. Yudhistira, and D. Hamdani, "Estimating the differential mode emission of a boost converter based on the input capacitor series resistance." *IEEE 7th Global Electromagnetic Compatibility Conference (GEMCCON), 2023,* doi: 10.1109/GEMCCON57842.2023.10078212.