Jurnal Elektronika dan Telekomunikasi (JET), Vol. 21, No. 2, December 2021, pp. 91-97
Accredited by RISTEKDIKTI, Decree No: **158/E/KPT/2021**
doi: 10.14203/jet.v21.91-97

Analytical Performance of Low Noise Amplifier Using Single-Stage Configuration for ADS-B Receiver

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Abstract

Automatic dependent surveillance-broadcast (ADS-B) is an equipment of a radar system to reach difficult areas. For radar applications, an ADS-B requires a low noise amplifier (LNA) with high gain, stability, and a low noise figure. In this research, to produce an LNA with good performance, an LNA was designed using a BJT transistor 2SC5006 with DC bias, VCE = 3 V, and current Ic = 10 mA, also a DC supply with VCC = 12 V, to achieve a high gain with a low noise figure. The initial LNA impedance circuit was simulated using two elements and then converted into three elements to obtain parameters according to the target specification through the tuning process, impedance matching circuit was used to reduce return loss and voltage standing wave ratio (VSWR) values. The LNA sequence obtains the working frequency of 1090 MHz, return loss of -52.103 dB, a gain of 10.382, VSWR of 1.005, a noise figure of 0.552, stability factor of 0.997, and bandwidth of 83 MHz. From the simulation results, the LNA has been successfully designed according to the ADS-B receiver specifications.

Keywords: LNA, ADS-B, single-stage.

I. INTRODUCTION

In recent years, rapid technological advances have driven new advances in various fields of science, especially in the field of radio communication. The development of radio communication is a serious concern of technological development in aviation navigation services [1], [2]. Flight navigation which initially used radar slowly began to shift to automatic dependent surveillance-broadcast (ADS-B) [3]–[6].

Automatic dependent surveillance-broadcast (ADSB) is a surveillance system in the avionics system of an aircraft, namely the MOD-S transponder [7], that automatically transmits a signal every 0.5 seconds or 2 times in 1 second.

The MOD-S transponder provides address, ident or squawk, latitude, altitude, nationality, speed, longitude, track, and heading information of aircraft. The MOD-S transponder on the aircraft receives location data from the GNSS (Global Navigation Satellite System) then forwards them to the ADS-B receiver.

A low noise amplifier (LNA) constitutes the ADS-B receiver system. LNA is used to amplify a signal with a small, fixed noise value. Parameters that need to be considered in designing the LNA are stability, gain, bandwidth, noise figure, return of loss, and voltage standing wave ratio (VSWR).

The current trend of LNA research is to use the right impedance matching circuit (IMC) L input matching circuit as the Pi matching circuit and the left IMC L filter output matching circuit to the T matching circuit.

A study of LNA design for the worldwide interoperability for microwave access (WIMAX) applications using 2.3 GHz radio-frequency with 0.35 um technology, that consumes a power of 1.656 mW at a supply voltage of 3.3 V [8]. Another study has attained perfect impedance match across the tuning range and has a stable operation of LNA design, which uses an inductively degenerated common source cascade amplifier to design the amplification stage, has attained a continuously tunable LNA design with a tuning range frequency from 2.2 to 2.8 GHz [9]. A proposed designed LNA was also applied for amplifying the weak signal at the front end of the receiver using PHEMT and GaAsFET in the geostationary satellite receiver system [10]. Research related to the implementation of LNA in the medical field was also carried out [11], which low noise operational amplifier dedicated to implantable biomedical applications is introduced using EKV Model to set the bias currents of the transistors. An LNA design has also been applied to the RF front-end receiver of a 2.45-GHz wireless communication system for IoT applications using the design proposed in [12], with the LNA adopting an architecture of power-constrained simultaneous noise and input matching based on the 0.18-µm CMOS process technology to achieve

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Received: March 20, 2021 ; Revised: September 2, 2021
Accepted: October 11, 2021 ; Published: December 31, 2021

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simultaneous noise and input matching at low power conditions. Another previous research regarding LNA was carried out with the design of low noise amplifier circuit in the L band frequency using a 0.18 nm CMOS transistor technology, which consists of two transistor stages for increase circuit linearization, creating an integrative matching network for system stability [13]. Studies of multiple LNA, aside from a single LNA, has also been carried out such as the use of multiband LNA for receiver system which is designed to work at 950 MHz, 1.8 GHz, 2.2 GHz, and 2.4 GHz center frequencies using HJ-FET NE32500 transistor which has self-bias characteristic through electronic design automation (EDA) simulations software [14]. Lastly, an approach for the design of narrowband cascaded and cascaded LNA with inductor source degenerated technique is presented for wireless body area network applications from [15].

This research was conducted by designing an LNA that works according to specifications to be applied to ADS-B receivers. In this research, it has been observed the following LNA parameters which are the return of loss, gain, VSWR, noise figure, stability, and bandwidth.

II. RESEARCH METHOD

The LNA specifications were designed to have a working frequency of 1090 MHz, return of loss < -10 dB, gain > 10, VSWR 1 ± 0.2, noise figure < 2, stability factor K > 1 and bandwidth > 10 MHz.

In this study, a BJT 2SC5006 transistor was selected and the characteristics are listed in Table 1 [16].

A. Block Diagram LNA

In this study, an LNA was designed using one active transistor, thus, a single-stage circuit configuration was chosen. The single-stage low noise amplifier consisted of 4 main parts, including the transistor itself as an amplifier, DC bias circuit, input circuit, and output matching as shown in Figure 1. A schematic single-stage amplifier is depicted in Figure 1. The block represents an active device (bipolar junction transistor) to maximize the DC input into the active transistor, which is influenced by the value of the resistor used in the DC bias circuit. Input and output matching networks are the pair

TABLE 1
THE CHARACTERISTICS OF THE 2SC5006 TRANSISTOR

PARAMETER	VALUE
Vce max	12 V
Ic max	100 mA
Noise Figure	< 1.5 dB
Gain	> 20
hFE	80 - 160

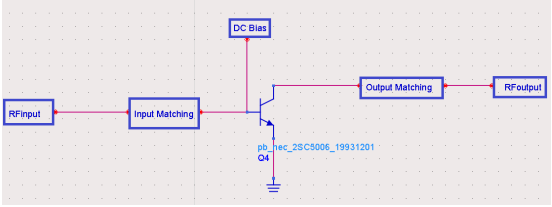

Figure 1. Block Diagram LNA.

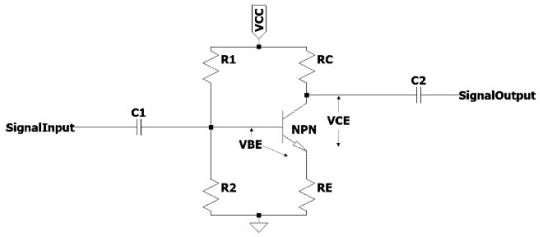

Figure 2. Voltage Divider Circuit [17].

of passive two-port networks in charge of matching the active device's terminals. The design of this LNA used the advanced design system (ADS) 2016 software.

In DC bias, a voltage divider circuit was used due to its excellent stability. The voltage divider bias circuit is displayed in Figure 2.

The voltage divider bias circuit in Figure 2 consists of four resistors, namely R1, R2, RC, and RE. Resistor R1 ensured the collector-base relationship is reverse biased, while resistor R2 ensured the base-emitter relationship is forward biased. Therefore, the presence of voltage dividers R1 and R2 guaranteed the transistor can work in the active region. RC as the collector load resistance, and RE as DC stabilization [17].

B. Transistor Working Point

Giving DC voltage bias to the transistor circuit was conducted to get a fixed voltage level and working current of the transistor. In a transistor amplifier, the constant voltage and current levels placed a working point on the characteristic curve, thus determining the working area of the transistor. Because the work point is a fixed point on the characteristic curve, it is called a Q-point or quiescent point.

The work point of an amplifier circuit could be located anywhere on the characteristic curve. For the amplifier circuit to linearly or flawlessly amplify the signal, the transistor's working point was placed in the middle of the active region. In addition, it was done so the work point is not placed outside the maximum limit of current or voltage that has been determined by the factory to protect the transistor from damage [18].

C. DC Bias

Amplifier circuits can multiply small AC input signals because they receive DC voltage from other sources. Therefore, every analysis and planning of the amplifier circuit has two components, namely AC and DC. Through the superposition theory, the DC and AC level conditions can be separated. The DC level of a circuit determines the working point of the transistor. There are two main considerations in designing a DC bias circuit, first, the bias circuit must be capable of providing one that does not affect changes in device parameters and temperature. Second, the bias circuit must be able to isolate the electric current from the high-frequency input so that the high-frequency current does not flow into the bias circuit [19].

The bias circuit in this design used a voltage divider, the planned target bias is VCE = 3 V and the current Ic = 10 mA with a DC supply VCC = 12 V. The values β =

100 and VBE = 0.8 V are obtained from the datasheet for voltage divider calculation process.

To determine the values of the 4 component resistors in the DC voltage divider bias circuit, we used (1) to (6).

$$V_E = 0.1 \times V_{CC} \quad (1)$$

$$V_B = V_{BE} + V_E \quad (2)$$

$$R_E = \frac{V_B}{I_C} \quad (3)$$

$$R_C = \frac{V_C}{I_C} \quad (4)$$

$$R_2 = 0.1 \times \beta \times R_E \quad (5)$$

$$R_1 = \frac{R_2 \times V_{CC}}{V_B} - R_2 \quad (6)$$

In Figure 3, there are additional components used for this bias circuit including DC Feed, DC Block, and capacitor. The use of DC Feed was to block the RF signal to hinder it disturbs the biasing conditions, then DC Block function was to ensure that the DC signal flow as a biasing of the transistor is maximized, and the capacitor was used as a short circuit when the RF signal flows so that the resistor on the emitter is not taken into account as the load of the transistor.

From the DC bias circuit in Figure 3, the results of the input impedance and output impedance are listed in Table 2.

D. Matching Impedance

The impedance adjustment aimed to reduce the return loss and VSWR results. In addition, the matching impedance improved transistor stability (K > 1). The initial series of input and output impedance matching in this research used the smith chart contained in the ADS software.

TABLE 2
THE RESULTS OF INPUT AND OUTPUT IMPEDANCE 2SC5006 TRANSISTOR

Impedance (Z)	Real + j*imaginer
Z_{in}	4.423 –j37.246
Z_{out}	20.568 –j124.390

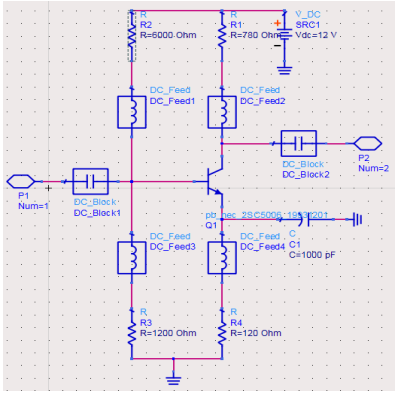

Figure 3. The DC Biasing Circuit for the 2SC5006 Transistor.

In Figures 4 and 5, left IMC L with a capacitor value of 3.64 pF at the impedance value (Z: 0.412-j2.488) was equipped for the input impedance circuit using the inductor 13.91 nH at the impedance has a value of (Z: 0.88+j1.162), the output impedance circuit used the right IMC L with an inductor value of 15.722 nH at the impedance value (Z: 0.142-j2.488), and the capacitor value of 6.983 pF is at the impedance value (Z: 0.088-j1.1629).

During the designing process, optimization of LNA parameters was also carried out by changing the configuration of the 2-element IMC circuit to 3-element IMC. The IMC input used the π type and the IMC output used the T type by adding a capacitor component. The value of the capacitor component then was changed to observe its effect on the VSWR, return loss, gain, and K factor parameters.

E. Return of Loss

The return of loss is a comparison between the amplitude value reflected against the transmitted amplitude or the amplitude increasing from the reflection to the energy compared to the transmitted energy. The return loss value also varies depending on the desired frequency, the reflection coefficient can be stated in (7).

$$\Gamma_L = \frac{V_o^-}{V_o^+} + \frac{Z_L - Z_o}{Z_L + Z_o} \quad (7)$$

Return of loss can occur due to the discontinuity between the transmission line and the input impedance. The amount of return of loss varies depending on the desired frequency. The return of loss value of –10 dB is generally acceptable since this value renders a

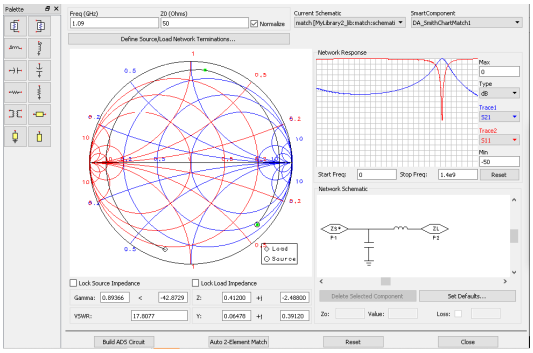

Figure 4. Input Matching Circuit.

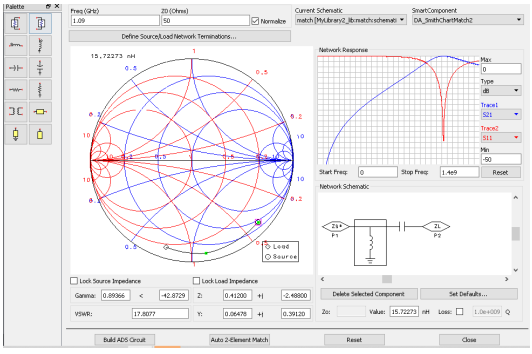

Figure 5. Output Matching Circuit.

significantly reduced reflected wave compared to the transmitted wave. This value also becomes a reference point to determine whether the antenna can work at the desired frequency [20].

F. Gain

Available Gain (GA = PAVN / PAVS) (8) is the ratio between the power on a two-port network and the power at the source [17].

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{|S_{11}|^2(1-|\Gamma_S|^2)}{|1-S_{11}\Gamma_S|^2(1-|\Gamma_{out}|^2)} \quad (8)$$

G. VSWR

Voltage standing wave ratio (VSWR) is the ratio between the standing wave amplitude for the maximum voltage (Vmax) and the minimum voltage (Vmin). Equation (9) was used to evaluate VSWR.

$$VSWR = \frac{V_{max}}{V_{min}} = \frac{1+|\Gamma|}{1-|\Gamma|} \quad (9)$$

The stress reflection coefficient has a complex value that represents the magnitude and phase of the reflection. Several cases define the following:

1. ΓL = -1 means the maximum negative reflection i.e when the channel is short connected.
2. ΓL = 0 means no reflections, *i.e.* when the channels are perfectly matched.
3. ΓL = +1 means the maximum positive reflection, *i.e* when the channel is connected in an open circuit.

The best condition is when the VSWR is 1, which means that there are no channel reflections in the perfect match [20].

H. Noise Figure

Noise is a problem for every system. Even in the absence of an input signal, noise still appears at the output. In an amplifier, the noise at the output is the input noise added to the noise generated by the amplifier itself. A large signal does not guarantee to provide a decent signal if followed by large noise. Signal to noise ratio or SNR states how big the signal is compared to the noise that occurs. There are two main sources of noise:

1. Thermal noise
   Thermal noise is the random fluctuation of the movement of electrons generated by heat in a conductor. If a noise resistor is the same as a load resistor, the mean thermal (heat) voltage squared at temperature T with bandwidth B is formulated in (10).

$$\overline{V_n^2} = 4KTBR_n \quad (10)$$

   Where K is 1.38×10^{-23} J/°K, T is the temperature (K), B is the bandwidth (Hz), Rn is the noise resistance (ohms).
2. Shot noise
   Shot noise is the fluctuation of the number of carriers in one current, and appears on all active devices. The mean shot noise current squares were calculated using (11).

$$\overline{I_n^2} = 2gI_{dc}B \quad (11)$$

   Where K is 1.38×10^{-23} J/°K, T is the temperature (K), B is the bandwidth (Hz), Rn is the noise resistance (ohms).

I. Stability

There are two main sources of noise.

1. Unconditionally stable

A circuit is said to be unconditionally stable if || Γin < 1 | (12) or | Γout < 1 | (13) for all passive sources and load impedances.

2. Conditional stable

A conditional circuit is stable if | Γin < 1 | (12) or | Γout < 1 | (13) only for a certain range of passive sources and load impedance and this case has the potential to be unstable [17].

$$|\Gamma_{in}| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}\right| < 1 \quad (12)$$

$$|\Gamma_{out}| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{11}\Gamma_L}\right| < 1 \quad (13)$$

J. Bandwidth

Bandwidth is an area where the LNA works properly. If an LNA works at a center frequency of f_c, it can still work properly at f_1 (below f_c) to f_2 (above f_c). Then, the bandwidth of the LNA is (f_1-f_2) with an increase in the VSWR value ≤ 2. The antenna bandwidth percentage is stated in (14) [20].

$$Bandwidth = \frac{f_H - f_L}{f_c} \times 100\% \quad (14)$$

Where f_c is frequency center (Hz), f_H is the high frequency (Hz), f_L is the high frequency (Hz).

III. Result and Discussion

Based on the initial DC bias circuit using the voltage divider circuit as shown in Figure 2, the simulation results of voltage and current are presented in Table 3.

Whereas in the LNA circuit, three optimization stages were carried out, at each optimization stage a circuit was changed and component value changes were carried out by tuning the ADS software. After obtaining the initial series of input and output matching using the smith chart as shown in Figures 4 and 5, the DC bias circuit and the impedance matching circuit were combined. From the initial series to the final optimization stage, changes in the parameters of return loss, gain, VSWR, noise figure, and stability factor were observed.

In the initial LNA circuit from combining DC bias circuits and impedance matching circuits obtained using

TABLE 3
THE RESULTS OF THE OBTAINED DC BIAS CURRENT AND VOLTAGE FROM SIMULATION

IB	IC	IE	VB	VC	VE
72.2118 µA	9.44205 mA	9.51426 mA	1.92779 V	4.6252 V	1.14171 V
VCE = VC - VE					3.482 V

the smith chart displayed in Figure 6, the results obtained are return loss parameters of -1.407 dB, a gain of -5.949, VSWR of 12.377, noise figure of 0.1777, and stability factor of 1.001 as shown in Figure 7. The results of the initial circuit did not meet the specifications, then

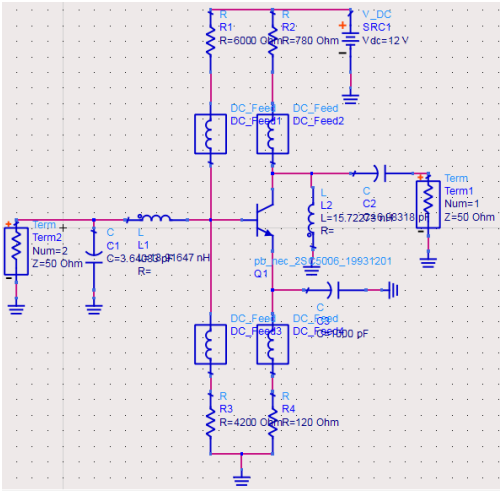

Figure 6. The Starting Circuit of the LNA.

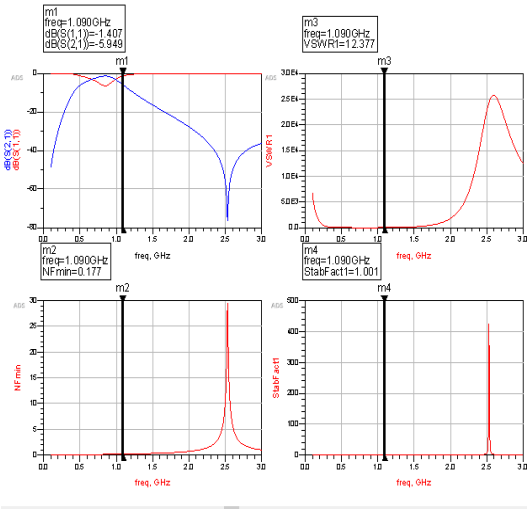

Figure 7. The Results of the Initial Circuit Parameters.

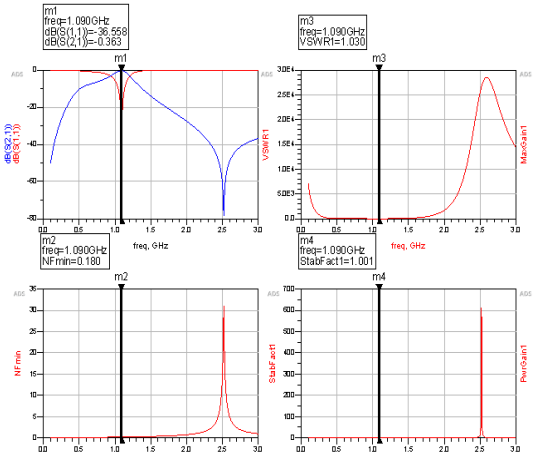

Figure 8. Results of Optimization Parameters 1.

optimization stage 1 was carried out by tuning the LNA circuit components, the results shown in Figure 8 are return loss parameters -36.558 dB, gain -0.363, VSWR 1.030, noise figure 0.180, and stability factor 1.001.

In the designed optimization 2 circuit as shown in Figure 9, changes were made to the input and output impedance matching circuit to a Pi matching circuit at the input and a matching T circuit at the output by adding a capacitor arranged in parallel to the input and a capacitor arranged in series at the output then tuning the overall LNA circuit components, the result The parameters obtained in the optimization stage 2 are return loss of -14.261 dB, a gain of -3.024, VSWR of 1.480, a noise figure of 1.269 and stability factor of 1.041. The results of optimization 2 still do not meet the targeted specifications as shown in Figure 10. Then the optimization stage 3 was carried out.

In optimization phase 3 as displayed in Figure 11, changes were made to the DC bias circuit by adding an inductor to the collector's foot, removing the resistors in the emitter and collector, and continuing the tuning process in the optimization LNA circuit 3. From the changes in optimization circuit 3, the parameter results shown in Figure 12 are return loss of -52.103 dB, a gain of 10.382, VSWR of 1.005, a noise figure of 0.552, and

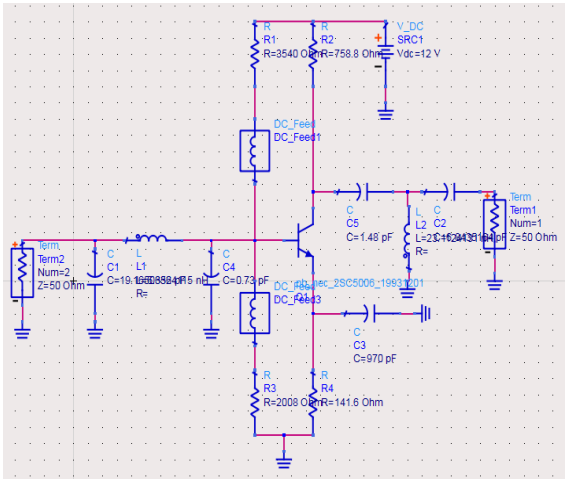

Figure 9. Optimization Circuit 2.

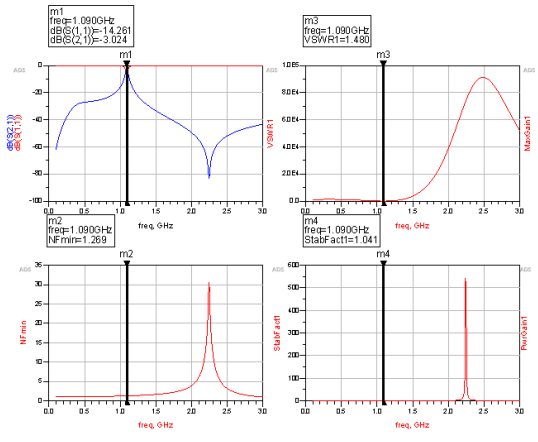

Figure 10. Results of Optimization Parameters 2.

stability factor of 0.997. At optimization stage 3, results that meet the targeted specifications are obtained.

Figure 13 shows m4 as the center frequency (f_c), m6 as the low frequency (f_l), and m7 as the high frequency (f_h). Using the calculation of (13) then the bandwidth value of 83 MHz is obtained.

From the three stages of optimization, the results of the LNA design are obtained from the simulation results that meet the targeted specifications. The results of the specifications obtained and the specifications of the targeted LNA are presented in Table 4.

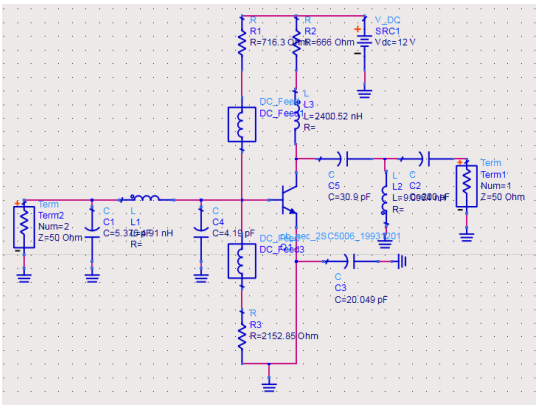

Figure 11. Optimization Circuit 3.

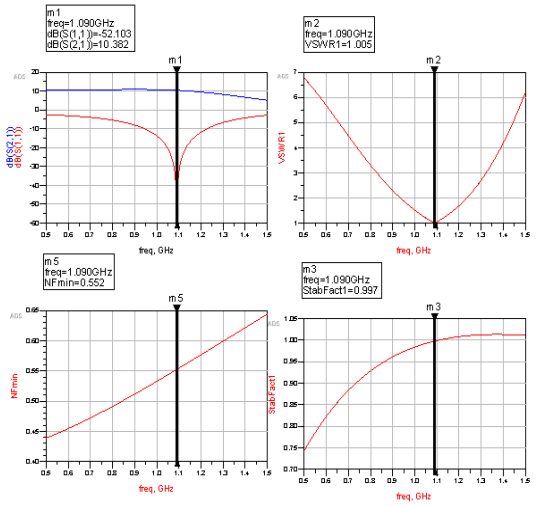

Figure 12. Results of Optimization Parameters 3.

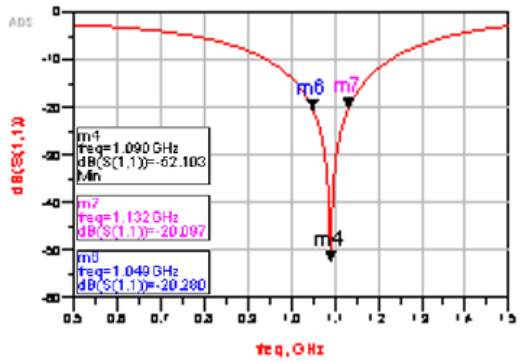

Figure 13. Measurement of Bandwidth in the Optimization Circuit 3.

TABLE 4
PARAMETER CHANGES OF THE INITIAL SERIES TO THE OPTIMIZATION STAGE 3

Parameter	Target Specification	Design Specification
Frequency Of Work	1.090 GHz	
Return of Loss	< -10 dB	-52.103 dB
Gain	> 10	10.382
VSWR	1 ± 0.2	1.005
Noise Figure	< 2	0.552
Stability Factor	K > 1	0.997
Bandwidth	10 MHz ± 2 MHz	83 MHz

CONCLUSION

Based on the optimization from simulation in stage 2, a change in the matching input series IMC L right low pass filter becomes a Pi matching circuit and the IMC L left high pass filter output matching circuit becomes a matching T series after changes are made and the tuning process is carried out on the component, the return loss value decreases from -36.558 dB to -14.261 dB, the original gain changes from -0.363 to -3.024 dB, VSWR increases from 1.030 to 1.480, the original noise figure increases from 0.180 to 1.269, and the stability factor increases from 1.001 to 1.041. Then the circuit change fails to optimize the parameters of the previous series, then continues to the optimization stage 3. In optimization stage 3, with the addition of inductors in the bias circuit and elimination of DC feed, resistors on the emitter and collector legs, and after tuning the components, results in parameters that meet specifications with a return loss value of -52.103 dB, a gain of 10.382, VSWR of 1.005, a noise figure of 0.552 and a stability factor of 0.997. In comparison with several previous studies where the LNA design focuses on the characteristics of the active component of the transistor, in this research, the addition of a passive component (capacitor) in the IMC circuit affects the parameters of the LNA and can be tuned as required. Future research should further build LNA that has been designed into hardware and conduct relevant measurements to confirm that the designed LNA works according to specifications.

ACKNOWLEDGMENT

We thank our fellow in Laboratory of Electrical Engineering Universitas Jenderal Achmad Yani which has provided support and guidance in this research.

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