

Fractional-N PLL Synthesizer for FMCW Signal Generator with Dual-Mode Modulation Pattern

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Abstract

Radar signal generator is a critical component in radar system as it determines the best achievable resolution. Single chip Fractional-N PLL synthesizer with built-in VCO and sweep modulator become more popular as Frequency Modulated Continuous Wave (FMCW) signal generator due to the simplicity and overall cost reduction. This paper presents a realization process and experimental result of dual-mode modulation pattern FMCW signal generator using HMC769LP6CE PLL. The PLL is controlled by ATMega328 microcontroller and Altera EPM240T100C5 CPLD to operate in two difference mode: 1-way sweep mode and 2-way sweep mode. The PLL is programmed with four different sweep bandwidth from 6.75–54 MHz for different range and resolution radar purpose. The performance of FMCW signal generator is measured using the output of passband signal spectrum. The experimental results indicate that the PLL-VCO with 2-way sweep mode has clearer frequency passband compared to 1-way sweep mode.

Keywords: FMCW, radar signal generator, PLL-VCO, sweep

I. INTRODUCTION

Many types of radars are used today for different types of applications and purposes. Frequency Modulated Continuous Wave (FMCW) radar is become popular due to the excellent detection characteristic at near ranges. The industry has started to discover this by using it in several commercial products. Some examples are collision detection radars for cars, altitude measurement and near obstacle ship navigation [1].

The capability of FMCW radar systems to achieve high receiver sensitivity and range resolution is directly relating to the phase noise and linearity of transmitter and receiver signal sources or oscillators [2]. Two architectures are particularly much use nowadays is the Direct Digital Synthesizer (DDS) and the Phase-Locked Loop (PLL) [3]. DDS integrated circuits (IC) support to generate precise linear frequency modulation (LFM) signals up to several hundred megahertz. However, for a high-frequency application, the output of DDS must be converted to radio frequency (RF) using several stages of up-converter. Those processes need some additional component (mixer, filter, oscillator, frequency pre-scaler, amplifier, etc.) that makes the system complicated and costly to develop. On the other hand, nowadays other types of frequency synthesizer IC that combine a Voltage Controlled Oscillator (VCO) with a PLL have been available in the market. The VCO is used to generate the RF, and the PLL is used to stabilize and control the frequency. The advantage of PLL-VCO

in FMCW radar system is the possibility to generate the LFM signal directly at RF frequency. This implementation will reduce overall system complexity, cost, and size.

Some researches have been done in the implementation of PLL-VCO in FMCW radar. A broadband millimeter wave VCO and HMC701LP6CE PLL are used to produce the broadband sweep generator for an 80 GHz radar system with 24.5 GHz bandwidth [4]. A highly linear and fully-integrated FMCW generator based on a fractional-N PLL and 60 GHz Colpitts VCO that can synthesize modulation schemes in 57–64 GHz range was proposed in [5]. A highly linear narrow band DDS with wideband VCO was used to generate ultra wideband FMCW sweep for Through-Wall Radar with 500-3000 MHz frequency bandwidth [6]. A frequency synthesizer for FMCW radars, operating in combination with a frequency multiplier, at 77 GHz, increases the target resolution and an improvement in the accuracy of the measurements of FMCW radars [7].

Within this paper, we present a realization process and experimental result of the dual-ramp mode FMCW signal generator using HMC769LP6CE PLL controlled by ATMega328 microcontroller and Altera EPM240T100C5 CPLD (Complex Programmable Logic Device) for marine radar navigation. The PLL is Fractional Fractional-N type PLL with built-in VCO with PLL-VCO configuration. The PLL is programmed to operate in two difference mode: 1-way and 2-way sweep mode. There is four difference sweep bandwidth configuration is used for different range and resolution which defines for low, medium, long and extra-long range detection. This design is simple to build, low-cost

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solution and easy to reconfigurable in the real-time operation for FMCW radar transmitter.

The rest of the paper is organized as follows. In section 2, the fundamental principle of FMCW radar and FMCW modulation pattern are presented. The detailed procedure for calculating register value to meet the different sweep bandwidth is presented in section 3. The measurement result of passband FMCW signal and detail timing signal recorded using spectrum analyzer (SA) and mixed digital oscilloscope (MDO) are presented in section 4. In the last section, we draw our conclusion.

II. FMCW RADAR SYSTEM

A. Basic FMCW Radar

FMCW radar takes the advantages of the continuous wave radars. Which is first the ability to employ high percentage duty cycles, that will yield high average transmitted power, but low peak power compared to pulsed systems. As the signal source of FMCW radar is continuously modulated, the radar is continuously operating by transmitting a modest power [8], [9]. The main hardware differences between pulse and FMCW radar are the pulse radars use magnetrons to generate the energy while FMCW uses solid-state oscillator and amplifiers. Moreover, pulse radars use a single antenna while an FMCW one uses two, one mounted on top of the other, generally in the same enclosure. The difference arises because pulse radars either transmits or receives at the different time slot while FMCW radar does both at the same time as shown in Figure 1.

B. FMCW Modulation Pattern

FMCW radar system transmits a continuous wave signal that is frequency modulated over a particular bandwidth. There are several possible modulation patterns, which can be used for different measurement purposes:

- Saw-tooth modulation (1-way sweep). This modulation pattern is used in a long-range (maximum distance) combined with a negligible influence of Doppler frequency (for example, a maritime navigation radar).
- Triangular modulation (2-way sweep). This modulation allows easy separation of the difference frequency (Δf) of the Doppler frequency (f_D).
- Square-wave modulation (simple frequency shift keying, FSK). This modulation is used for a precise distance measurement at close range by phase comparison of the two echo signal frequencies. It has the disadvantage, that the echo signals from several targets cannot be separated from each other, and that this process enables only a small unambiguous measuring range.
- Stepped modulation (staircase voltage). This modulation is used for interferometric measurements and expands the unambiguous measuring range.

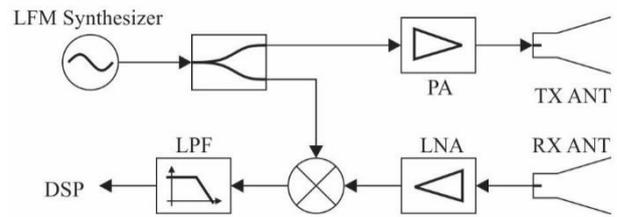


Figure 1. Basic FMCW radar block

The typical sweep modulation of FMCW is linear FM (LFM) as shown in Figure 2. The bandwidth of this signal determines the radar range resolution. The broad bandwidth produces high range resolution, as given by

$$\Delta R = \frac{C}{2B} \quad (1)$$

in which ΔR is radar range resolution, C is free space speed of light and B is radar signal bandwidth.

III. EXPERIMENTAL AND METHOD

A. Generating LFM Signal Using Fractional-N PLL Synthesizer

The default modern Phase Locked Loop (PLL) comprises a reference source, a phase frequency detector, a charge pumps (CP), a loop filter, and a voltage controlled oscillator (VCO). Figure 3 shows a typical block diagram of a PLL with variable pre-scaler R and N . The PLL circuit performs frequency multiplication, via a negative feedback mechanism, to generate the output frequency. The output of the VCO is phase compared with the input reference at the phase frequency detector (PFD), which the phase of a generated signal is forced to follow that of a reference signal. When the loop reaches lock condition, the frequency of the generated signal (f_{VCO}) is also equal to that of the reference (f_{ref}) [10] - [11].

$$f_{VCO} = \frac{f_{ref}}{R} N \quad (2)$$

This traditional digital PLL implementation will be termed “integer-N” to avoid confusion due to the addition of fractional-N technology.

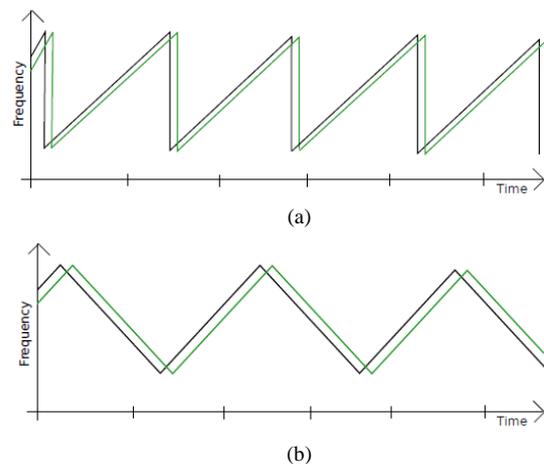


Figure 2. LFM signal (a) saw-tooth modulation (b) triangular modulation.

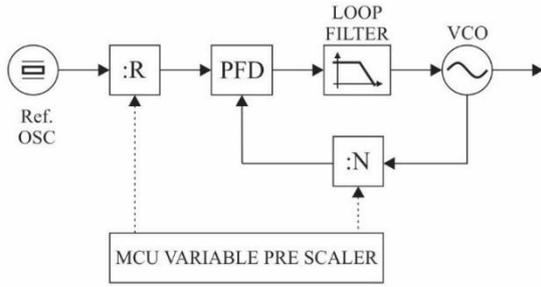


Figure 3. Integer-N PLL with variable pre-scaler.

The term "fractional-N" describes a family of synthesizers that allow the minimum frequency step to be a fraction of the reference frequency. A newly emerging PLL technology has made it possible to alter the relationship between N , f_{ref} , and the channel spacing of the synthesizer. This is accomplished by adding internal circuitry that enables the value of N to change dynamically during the locked state. If the value of the divider is "switched" between N and $N+1$ in the correct proportion, an average division ratio can be realized that is N plus some arbitrary fraction, k/M . This allows the phase detectors to run at a frequency that is higher than the synthesizer channel spacing [12], as given by

$$f_{VCO} = f_R \left(N + \frac{k}{M} \right) \quad (3)$$

$$f_R = \frac{f_{ref}}{R} \quad (4)$$

where k and M are integers. M is a measure of the fractionality that a fractional-N synthesizer can provide. It is usually referred to as "fractional modulus" or "fractional denominator." k can assume any number between 0 and M . The non-integer number $(N+k/M)$ is often written as $N.F$, where the dot denotes a decimal point, and N and F represent the integer and fractional parts of the number, respectively.

In this project, we used Analog Device HMC769LP6CE Fractional-N PLL chip to generate LFM signal. The HMC769LP6CE is a fully functional Fractional-N Phase-Locked-Loop (PLL) Frequency Synthesizer with an integrated VCO [13]. The range of frequency input reference (reference oscillator) is from DC to 350 MHz while the advanced delta-sigma modulator design in the fractional synthesizer allows ultra-fine step sizes for generating LFM signal sweep. Integrated VCO is capable of generating RF signals in the frequency range from 9.05 GHz to 10.15 GHz. Also, the HMC769LP6CE offers frequency sweep and modulation features, external triggering, double-buffering and precise frequency control. These features very useful to generate reconfigurable LFM signal during radar operation in real time, by configuring chip register using serial interface using a microcontroller.

B. System Design

To simplify our design process, we use HMC769LP6CE evaluation board, which equipped with 50 MHz reference oscillator and onboard loop filter [13]. 9.3 GHz is used as the center frequency to meet

maritime radar requirements of IMO MSC 192/5.1.2. The radio regulations and applicable ITU-R recommendations for maritime radar frequency allocation in X-band (9.2 to 9.5 GHz).

Two different sweep modes are used in our system: 1-way sweep mode and 2-way sweep mode. In the 1-way mode, the sweep will linearly increase (ramp-up) from low frequency (f_L) to high frequency (f_H) during a specific period (t_{sweep}). The sweep will hop back to initial frequency (f_L) before the next sweep begins. A proper time guard (t_{guard}) must be inserted to ensure the sweep settle back after the broad frequency hop. In the 2-way mode, the frequency will ramp-up from f_L to f_H in the first period of t_{sweep} and ramp-down from f_H to f_L in the second period of t_{sweep} . The precise timing diagram of the sweep is showed in Figure 4 and parameterized in Table 1.

To generate the RF signals using the HMC769LP6CE chip, we need to set up some of the internal control registers of PLL using the appropriate parameter with the desired RF signal. The PLL is configured using a microcontroller which has Serial to Parallel Interface (SPI) to PLL and Universal Serial Bus (USB) interface to the PC. 50 MHz crystal oscillator is used as a primary reference to maintain the signal coherency. The signal is split respectively as a reference signal source for PLL and synchronization signal source for PLL triggering circuits. PLL trigger generated by dividing 50 MHz signals using complex programmable logic device (CPLD) chip. This signal is used to trigger the sweep to start, which in radar term known as sweep radar interval. CPLD also used to generate coherent signal clock and triggering for Analog to Digital Converter (ADC) to sampling the beat signal. Simplified schematic diagram of each component is shown in Figure 5.

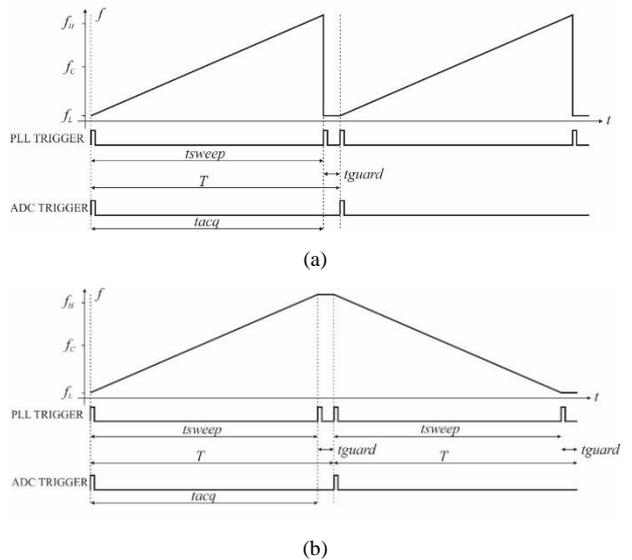


Figure 4. Frequency sweep timing diagram. (a) saw-tooth modulation (b) triangular modulation.

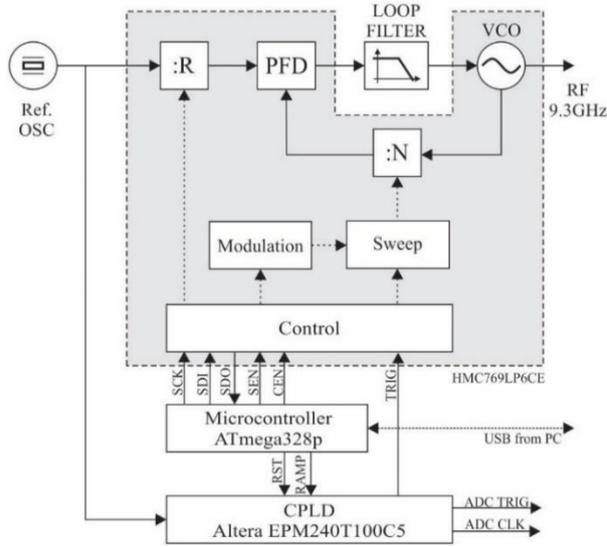


Figure 5. Simplified schematic diagram of a realization of fractional-N PLL for FMCW radar.

C. Sweep Configuration

The design specification of FMCW marine radar navigation system is summarized in Table 1.

There are four different sweep bandwidth configuration used for different range and resolution of radar imaging, that defines as low, medium, long, and extra-long range detection. The correlation between each sweep bandwidth with desired radar range and resolution showed in Table 2.

1) Programming PLL Register

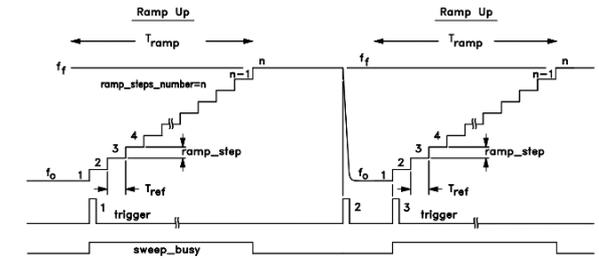
There are total 20 registers (Reg00h...Reg14h) that should be programmed carefully to configure PLL as FMCW signal generator according to the Table 1 specification.

TABLE 1
DESIGN SPECIFICATION OF LFM RADAR SIGNAL

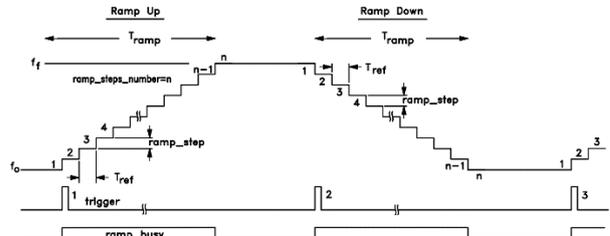
Parameter	Value	Unit
Center Frequency	9.3	GHz
Antenna rotation	24	rpm
Integration Number	8	
Chirp Repetition Interval (T)	1000.32	μ s
Sweep Time (t_{sweep})	983.04	μ s
Guard Time (t_{guard})	17.28	μ s
Azimuth Resolution	1.152	deg
Frequency Sampling	2.0833	MHz
Frequency Beat Maximum	2.0833	MHz
Range Gate	2048	
Azimuth Gate	312.4	

TABLE 2
THE CORRELATION BETWEEN SWEEP BANDWIDTH AND RANGE

	BW (MHz)	f_L (MHz)	f_H (MHz)	R_{res} (m)	R_{max} (Nm)
Short	54	9273.00	9327.0	2.78	3.08
Medium	27	9286.50	9313.5	5.57	6.15
Long	13.5	9293.25	9306.8	11.13	12.31
Extra Long	6.75	9296.63	9303.4	21.33	23.59



(a)



(b)

Figure 6. (a) 1-way and (b) 2-way sweep frequency modulation as LFM generator [14].

The HMC703LP4E can be configured to operate in 1-way triggered sweep mode, and 2-way triggered sweep mode as shown in Figure 6. The start of the sweep is triggered by inserting logic “high” from PLL triggering circuits to external TRIG pin number 6 to keep synchronized with data acquisition processor and another module. Triggered 1-way sweeps also require a third trigger to start the new sweep. The third trigger should time appropriately to allow the VCO to settle after the broad frequency hop back to the start frequency [14].

The following procedure is taken to configure sweep for short-range radar operation according to the specification given in Table 2. The sweep start from $f_L = 9273$ MHz to $f_H = 9327$ MHz. A 50 MHz crystal oscillator is used as a frequency reference, $f_{\text{ref}} = 50$ MHz, with sweep time ($T_{\text{sweep}} = 983.04$ μ s).

- Lock in fractional mode to the start frequency (f_L).
Reg 06h[7:5] = 0.
- Set 50 MHz frequency reference (f_{ref}) as frequency of Phase Detector (f_{PD}). Reference divider register (R) = 1.
Reg02h[13:0] = 1.
- Set RF divider register (N_{RF}) as additional loopback divider to 4.
- Calculate N_{Start} and N_{Stop} , using start and stop frequency, (f_L and f_H).
 $N_{\text{Start}} = 9273.0 \text{ MHz} / 50.0 \text{ MHz} / 4 = 46.365$.
 $N_{\text{Stop}} = 9327.0 \text{ MHz} / 50.0 \text{ MHz} / 4 = 46.635$.
- Set Start N register, Reg03h as integer part and Reg04h as fractional part.
Reg03h = 46d = 0x00002Eh.
Reg04h = $0.365 \times 2^{24} = 0.365d = 0x5D70A3h$.
- Calculate how many reference cycles will occur during sweep time, $T_{\text{sweep}} \approx 983.04$ μ s.
Given that $T_{\text{ref}} = 1 / f_{\text{PD}} = 20$ ns.
 $\text{NbrOfSteps} = T_{\text{ramp}} / T_{\text{ref}} = 983.04 \mu\text{s} / 20\text{ns} = 49152$.
- Calculate the desired N_{step} size, given N_{Start} , N_{Stop} and NbrOfSteps .

$$N_{Step_Size_desired} = (46.365 - 46.635) / 49152 = 5.493\mu \text{ (fractions of } N\text{)}.$$

8. Quantize the fractional N_{step} into the 24 bit step size. $Reg0Ah = 5.493\mu \times 2^{24} = \text{round}(92.157) = 92d = 0x5Ch$.
9. Readjust the stop frequency slightly to ensure it falls exactly on a step boundary.
Sweep time = 49152 cycles = 983.04us.
 $N_{Stop} = N_{Start} + NbrOfStep \times N_{step} / 2^{24}$.
 $N_{Stop} = 46.365 + 49152 \times 92 / 2^{24} \approx 46.634531$
10. Set Stop N Register, Reg0Ch as Integer part and Reg0Dh as Fractional part.
Reg0Ch = 46d = 0x00002Eh
Reg0Dh = $0.634531 \times 2^{24} = 0.634531d = 0xA270A3h$.
11. Set SD_Mode register to Sweep-1way-Ramp then hop (Triggered) for 1-Way sweep mode.
Reg06h[7:5] = 5.
or program SD_Mode register to Sweep-2way-Ramp for 2-Way sweep mode.
Reg06h[7:5] = 6.
12. Program trigger via an external pin.
Reg06h[9] = 1.
13. Continue to issue triggers to advance the ramp profile to the next stage.

Note that the ramp step Reg0Ah is signed two's complement. If negative integer exists, the first ramp has a negative slope, and vice-versa. Set the auto seed register (Reg 06h[8] = 1) to ensure the different sweeps have same phase profile. Moreover, loading the seed value 0x0h into the phase accumulator (Reg 05h) at the beginning of each ramp. Also, setting Reg06h[22] = 1 to ensure the same phase and quantization noise performance on each sweep by resetting the entire delta-sigma modulator at the beginning of each ramp.

The other register value that should be programmed for the different radar range resolution are shown in Table 3, and the correlations between each register with start frequency and stop frequency are shown in Table 4. There is a shift in frequency and bandwidth arising from the calculation process of the registers.

2) Timing Generator

Altera EPM240T100C5 is used as timing generator to generate PLL trigger. Figure 7 shows a simplified block diagram of timing generator. 50 MHz clock source obtained from the same crystal oscillator used by PLL reference frequency is divided by 48, by two cascade divider by 6 and divider by 8, to generates 1.041667 MHz clock with a period of 0.96 μ s. The 1024 binary clock counter which is clocked by 1.041667 MHz clock generates a pulse at counter time 0, 1024 and 1042(=0). The counter will reset at count 1041, generating 983.04 μ s sweep time, 983.04 μ s guard time and 1000.32 μ s sweep repetition period. An external input selector which is controlled by microcontroller inserted into CPLD circuits to disable the second trigger that not used in 2-way sweep mode to hop back the frequency to initial frequency. Logic '0' will enable the second pulse (trigger for 1-way sweep) and logic '1' will disable the second pulse (trigger for 2-way sweep).

TABLE 3
REGISTER VALUE FOR DIFFERENT SIGNAL BANDWIDTH

	N_{start}		N_{step}	N_{stop}	
	Int	Frac		Int	Frac
	Reg03h	Reg04h	Reg05h	Reg0Ch	Reg0Dh
Short	2E	5D70A3	5C	2E	A270A3
Medium	2E	6EB851	2E	2E	913851
Long	2E	775C28	17	2E	889C28
Extra Long	2E	7BAE14	0C	2E	84AE14

TABLE 4
SHIFTED START AND STOP (BANDWIDTH) FREQUENCY

	BW(MHz)	f_L (MHz)	f_H (MHz)
Short	53.906250	9272.999990	9326.906240
Medium	26.953125	9286.499989	9313.453114
Long	13.476563	9293.249989	9306.726551
Extra Long	7.031250	9296.624994	9303.656244

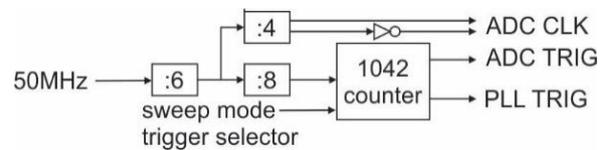


Figure 7. Timing generator based Altera CPLD.

For ADC triggering purpose, just the initial pulse generated at counter count = 0 used as ADC trigger to start data acquisition and guarantee ADC and PLL have the same initial time reference (synchronous). ADC clocked using frequency sampling of 2.083333 MHz that obtained from dividing 50 MHz clocks using divider by 24. That will produce 2048 sample for every 983.04 μ s sweep time (2048 range gate).

IV. RESULT AND DISCUSSION

This section presents the results of signal measurements produced by PLL-VCO as a chirp generator. Figure 8 shows recorded clock and triggering signal. The signals probe using Tektronix MDO3012 Mixed Domain Oscilloscope. The Channel 1, 2, and 3 of MDO screen shows PLL Trigger, ADC Trigger, and ADC Clock respectively. The measurement result for chirp repetition period is 1.000 ms, and ADC clock is 2.083 MHz. The results of chirp repetition period is slightly shifted from predetermined specifications, which is 1000.32 μ s. The main difference between Figure 8(a) and 8(b) is in channel 1 (PLL Trigger) is a second pulse generated to trigger PLL to hop back to the start frequency before starting to the next ramp.

Channel 4 is PLL loop filter output, which is used as VCO control voltage in the PLL-VCO circuits. The form of the control voltage is saw-tooth for 1-way sweep and triangle for 2-way sweep as shown in Figure 8(a) and 8(b) respectively. These results confirm that PLL was successfully swept the VCO and generate frequency output from low frequency (f_L) to high frequency (f_H), and vice versa, for both modes. The slope of control voltage defines how fast VCO frequency changes with time and confirmed that start and stop of the ramp are synchronous with PLL trigger.

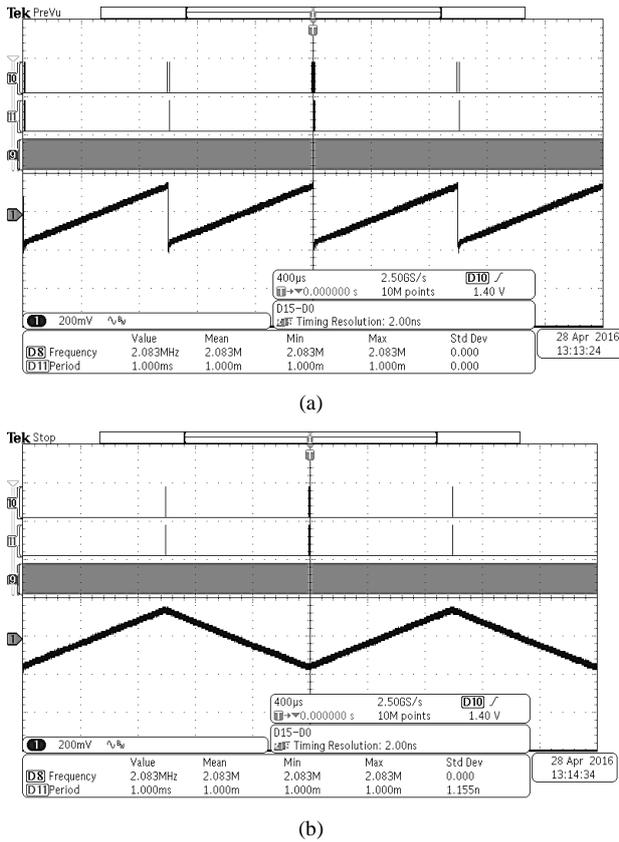


Figure 8. Trigger, clock and VCO control voltage (a) 1-way sweep (b) 2-way sweep.

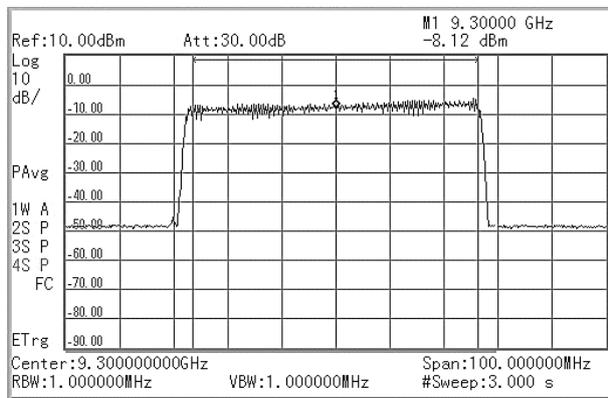
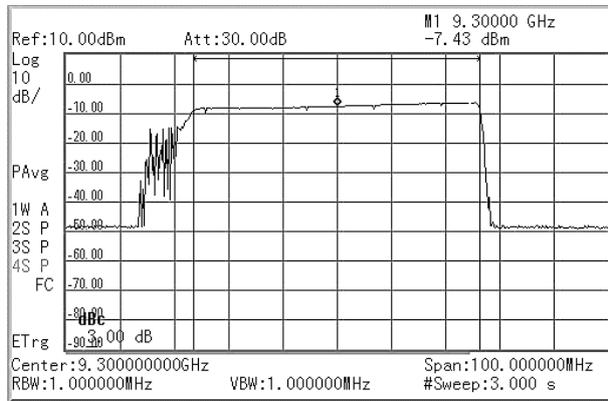


Figure 9. The spectrum of measured LFM chirp for short-range detection (a) 1-way sweep (b) 2-way sweep.

The measured spectrum of LFM chirp for short-range detection (53.9 MHz bandwidth) shown in Figure 9. The measurement performs by connecting output of RF port PLL-VCO to Keysight N9343C spectrum analyzer. The series of measurements also performed for different chirp bandwidth specification, 26 MHz, 13.26 MHz and 6.75 MHz respectively, with 9.3 GHz center frequency. For every chirp specification, the microcontroller sends out appropriate N_{start} , N_{stop} and N_{step} register through SPI interface of HMC769LP6CE PLL according to value from Table 3.

The performance of chirp spectrum summarized in Table 5. Bandwidth is measured using 99% of power level, and the spectrum flatness is measured using power level difference between start and stop frequency. For overall chirp signal, the passband response (spectrum flatness) is less than 3 dBm.

The spectrum of single tone signal at 9.3 GHz is shown in Figure 10. The output power is about 9.04 dBm, 3 dB less that datasheet specification (12 dBm), but is still acceptable due to connector and cable loss. The highest spurious level is -48 dBm (57 dBc) at 400 MHz offset. Noise floor measured around 98 dBc. Both of these spurious and noise floor levels are acceptable for the proper functioning of the RF system (at least 40 to 50 dBc).

TABLE 5
MEASURED CHIRP PERFORMANCE

	Parameter	Value	Unit
Short	Bandwidth	53.04	MHz
	Power Level @9.3GHz	-7.43	dBm
	Spectrum flatness	2.2	dBm
Medium	Bandwidth	26.52	MHz
	Power Level @9.3GHz	-4.32	dBm
	Spectrum flatness	1.7	dBm
Long	Bandwidth	13.26	MHz
	Power Level @9.3GHz	-1.49	dBm
	Spectrum flatness	0.6	dBm
Extra Long	Bandwidth	6.73	MHz
	Power Level @9.3GHz	1.60	dBm
	Spectrum flatness	0.2	dBm

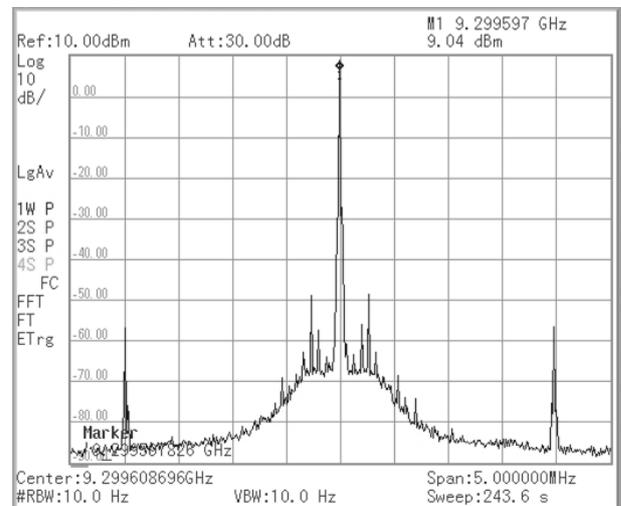


Figure 10. Spectrum purity of single tone at 9.3 GHz.

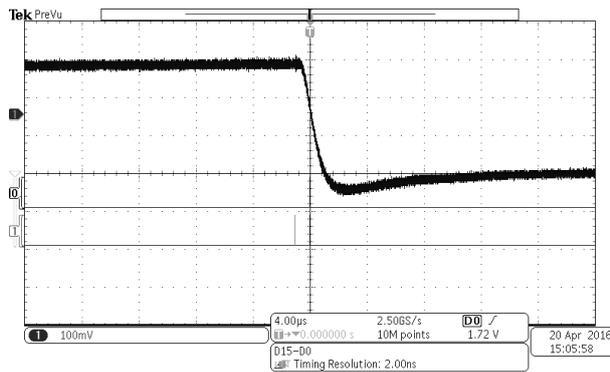


Figure 11. Control voltage overshoot during broad frequency hop

As shown in Figure 9(a), there is an additional spectrum on the left side of desired passband ramp signal. The additional frequency spectrum comes from broad frequency hop at the end of sweep frequency during back to initial sweep frequency that can be seen in Figure 11. Overshoot control voltage that arises below initial control voltage value resulting an additional spectrum below passband. The VCO voltage control signal measured using 54 MHz bandwidth configuration, the highest frequency sweep design. Due to this condition, at least 15 μ s guard time must be inserted for PLL to hop back to initial frequency before start to the next sweep.

In our design, the additional spectrum during guard time avoided/rejected for transmission using bandpass filter before the signal is amplified and transmitted from the antenna. In radar signal processing process, we carefully reject the beat signal (FMCW receive signal) during data acquisition. The signals sampled during the time guard period are ignored in the signal processing process.

Besides the capability of HMC769LP6CE PLL to generate FMCW LFM signal to meet our purpose, the spectral purity and additional spectrum outside passband due to control voltage overshoot must be improved in 1-way sweep mode. The loop filter must be investigated and modified (redesign) to reduce the control voltage overshoot. 2-way sweep mode ramp produces better passband spectrum without additional spectrum (bandwidth) and overshoot problem. Some of supporting circuit that contributes to noise performance of PLL-VCO architecture must be improved, i.e., power supply, digital logic connection, etc.

CONCLUSION

A Fractional-N PLL-VCO based FMCW radar chirp generator with dual pattern modulation capability has been designed and experimentally tested. HMC769LP6CE PLL with internal sweep modulator and Integrated VCO is suitable for linear frequency modulation and easily controlled by programming binary code with different bandwidth setup. A VCO in the PLL is useful to cover wideband operation and generate a signal directly in RF frequency. Thus, the combination of a VCO and a PLL is suitable for wideband linear modulation. Moreover, we have shown the detailed design procedure to calculate and setup

register of HMC769LP6CE PLL as FMCW radar chirp generator, controlled by ATMega328 microcontroller and Altera EPM240T100C5 CPLD. HMC769LP6CE PLL reduces overall system cost, design complexity, and solution size by integrating a VCO with PLL components, including a reference divider, phase-frequency detector, low noise charge pump, fractional divider and VCO output divider and buffer. These combined specifications make the HMC769LP6CE suitable for wide range applications, such as wireless communications using complex modulation schemes, communications systems that employ long burst durations and radar transceiver.

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